Non-Backflow-Power and Reduced-Switching-Loss Modulation for Bidirectional Series Resonant Converter With Wide Gain Range

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Abstract—In the achievement of high power efficiency over a wide gain range for a bidirectional series resonant converter (BSRC), conduction losses caused by backflow power and switching losses are two challenges. In this article, a novel modulation of the BSRC is proposed for a wide voltage gain range and high efficiency as well. With the proposed modulation, the BSRC can operate in both buck- and boost-like modes for a wide gain range. The resonant current is in phase with the terminal voltage on both primary and secondary sides, to eliminate the backflow power for the reduction of conduction losses. Hard turn-off problem is alleviated with a resonant current fully released before the completion of the switching cycle. Thus, the number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature. A control scheme based on state-flowchart is also proposed to realize seamless transition among different working modes. To validate the proposed modulation, a 1 kVA prototype of BSRC is developed and interfaces a high-voltage bus ranging from 240 to 480 V and a low-voltage bus ranging from 24 to 56 V. Compared with conventional modulation schemes, efficiency enhancement can be observed over the whole operating range.

Index Terms—Bidirectional series resonant converter (BSRC), discontinuous current mode (DCM), non-backflow-power, reduced-switching-loss, zero current switching.

I. INTRODUCTION

BIDIRECTIONAL DC–DC converters are attracting more and more attention due to the rapid development of renewable energy sources, battery storage system, DC grids, electric vehicles (EVs), and so on. They can operate as an interface between a high-voltage bus installing energy generation devices, grid-connected converters or loads, and a low-voltage bus where energy storage devices are loaded [1]. In most of these applications, bidirectional power flow between the two buses requires high power efficiency over a wide gain range, which is still challenging the design and modulation of the DC–DC converters [2], [3], [4], [5].

Characteristics of unidirectional LLC resonant converters have been widely studied, and some studies propose bidirectional LLC resonant converters [6], [7], [8], [9]. However, in the reverse mode, the LLC resonant converter is equivalent to an LC series resonant converter, leading to a diverse gain feature compared with the forward mode. Although an auxiliary inductor can be added between the primary full-bridge circuit and the LLC resonant tank for symmetric behaviors [10], the converter suffers from the increase in power loss and component cost. Instead of using an auxiliary inductor, a resonant capacitor can be added to the secondary side of the LLC resonant tank [11], but the behaviors of the forward mode and the reverse mode are still asymmetric due to the unmatched capacitor values. Then, Jung et al. [12], Malan et al. [13], Zhang et al. [14], and He et al. [15] propose a symmetric CLLC resonant tank for the bidirectional DC–DC converter to achieve symmetric behaviors in the forward and reverse modes. The asymmetric problem can be addressed by adding proper components to the existing LLC resonant tank, but there exist obvious penalties that include the use of more components, the increase in component cost, and the decrease in power density.

With the simplest and symmetric circuit topology of the resonant tank, bidirectional series resonant converters (BSRCs) are worth investigating [16], [17], [18], [19], [20]. Compared with the CLLC resonant converter, the resonant tank of the BSRC is greatly simplified from \( L_1 \)–\( L_2 \)–\( L_m \)–\( C_1 \) to \( C_1 \)–\( L_r \), while symmetric behaviors can still be maintained by ignoring the large magnetic inductance. In general, the BSRC has four degrees of control freedom, including primary duty cycle \( D_p \), secondary duty cycle \( D_s \), shifting phase between the primary and the secondary \( \phi \), and switching frequency \( f_s \). Typical modulation schemes can be configured based on these basic control variables, as highlighted in Table I for comparison.

Variable frequency modulation (VFM) changes the switching frequency \( f_s \) to regulate the output power [11], [15], [21], achieving zero voltage switching (ZVS)-ON for primary
TABLE I

COMPARISON OF MODULATION SCHEMES FOR BSRC

<table>
<thead>
<tr>
<th>Modulation</th>
<th>Control degree</th>
<th>Operating range</th>
<th>Backflow power</th>
<th>Soft switching</th>
<th>Power</th>
<th>Efficiency of full power output</th>
<th>Operating frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFM [11], [15], [21]</td>
<td>$f_s$</td>
<td>Narrow</td>
<td>Medium: backflow power at input side</td>
<td>Good: 4 ZVS-ON and 8 ZCS-ON/OFF actions for full range</td>
<td>500VA</td>
<td>95%</td>
<td>73kHz-131 kHz</td>
</tr>
<tr>
<td>PSM [13], [17], [22]</td>
<td>$\phi$</td>
<td>Wide</td>
<td>Large: backflow power at both side</td>
<td>Medium: 8 ZVS-ON actions for high power range</td>
<td>200VA</td>
<td>95%</td>
<td>100kHz</td>
</tr>
<tr>
<td>PSM + PWM [23]–[31]</td>
<td>$\phi$, $D_p$</td>
<td>Wide</td>
<td>Small: no backflow power</td>
<td>Poor: no more than 8 ZVS-ON actions for high power range</td>
<td>1000VA</td>
<td>95%</td>
<td>500kHz</td>
</tr>
<tr>
<td>VFM + PSM [18]</td>
<td>$\phi$, $f_s$</td>
<td>Wide</td>
<td>Medium: backflow power at output side</td>
<td>Good: 8 ZVS-ON actions for full range</td>
<td>800VA</td>
<td>94.8%</td>
<td>41.3 kHz</td>
</tr>
<tr>
<td>FDM [32], [33]</td>
<td>$\phi$, $D_p$, $D_s$</td>
<td>Wide</td>
<td>Small: no backflow power</td>
<td>Medium: 8 ZVS-ON actions for high power range</td>
<td>1000VA</td>
<td>94%</td>
<td>100kHz</td>
</tr>
<tr>
<td>VFM + PWM (Proposed)</td>
<td>$f_s$, $D_p$</td>
<td>Wide</td>
<td>Small: no backflow power</td>
<td>Good: 14 soft-switching actions for full range</td>
<td>1000VA</td>
<td>96%</td>
<td>50kHz-200kHz</td>
</tr>
</tbody>
</table>

switches over a full operating range as shown in Fig. 1(a). However, there exists backflow power on the input side as indicated by the green area, which will increase conduction losses in the primary switches. Moreover, due to the series LC-type resonant network, the narrow operating range is another concern of VFM. To address this challenge, phase shift modulation (PSM) is proposed in some studies [13], [17], [22]. By adjusting the shifting phase $\phi$ between the primary and secondary, the output power can be regulated over a wide voltage-gain range. However, two issues brought by PSM degrade the efficiency: a) soft switching cannot be maintained at light load and b) backflow power exists in both the primary and the secondary, resulting in a large circulating current.

In order to minimize the resonant current, pulsewidth modulation (PWM) of $D_p$ and $D_s$ is used to reduce the reactive currents, while the PSM of $\phi$ is responsible for regulating the delivered power [19], [20], [23], [24], [25]. The modulation scheme can be named as PSM + PWM. Zero voltage level can be inserted in the full-bridge circuit to block the backflow power in both the primary and the secondary to minimize the resonant current. However, the switches suffer from hard turn-on and turn-off, as shown in Fig. 1(b), resulting in significant switching losses. Some modified PWM and PSM schemes are proposed [26], [27], [28], [29], [30], [31] to reduce the switching loss, but at the cost of backflow power. Moreover, soft switching may fail in some light load conditions in these modulation schemes. Another hybrid modulation based on VFM and PSM (VFM + PSM) is proposed in [18] to achieve ZVS for the whole operating range, showing that VFM + PSM has better efficiency performance because of the reduction in the switching loss. However, the resonant current is only in phase with the terminal voltage on the primary side, which means the backflow power still exists in the secondary.

Extra control freedom can be offered by adding VFM to PSM and PWM, which can also be named as four-degrees-of-freedom modulation (FDM). Based on fundamental approximation, a complex closed-form solution of $f_s$, $D_p$, $D_s$, and $\phi$ can be derived for the elimination of backflow power by making the resonant current in phase with both the primary and secondary terminal voltages [32], [33]. However, a fundamental approximation cannot describe the converter features accurately when the switching frequency is away from the resonant frequency or the duty cycle is far smaller than 0.5. Therefore, in medium or light load conditions,
backflow power cannot be eliminated. Moreover, complex calculations are used in this method to simultaneously regulate the four variables, which are difficult to be realized in practice. Therefore, the proposed method in this article only compares with the VFM + PSM method.

Although VFM + PSM can achieve ZVS turn-on, it does not take into consideration hard switching during the turn-off process, which should not be ignored especially when the turn-off current is large. Therefore, we are motivated to develop a novel modulation scheme that aims to achieve high overall efficiency with backflow power being eliminated and switching losses being optimized, as shown in Fig. 1(c).

In this article, a non-backflow-power and reduced-switching-loss modulation is proposed for the BSRC to achieve high overall efficiency within a wide gain range. The contributions of this article as follow.

1) Soft switching features are achieved not only for switch-ON but also for switch-OFF. More than 14 out of the total 16 (14/16) switching actions can realize soft switching for the full range. The number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature.

2) Backflow power is both eliminated at the input and output sides.

3) Wide gain range is adjusted for the BSRC operates in buck- and boost-like modes similar to the operation of buck and boost DC–DC converters.

The rest of the article is organized as follows. Section II illustrates the proposed modulation in detail. The output characteristic and control scheme are analyzed in Section III. Section IV takes into consideration design issues on rms resonant current and soft switching. Experimental verification is given in Section V. Finally, Section VI concludes the article.

II. PROPOSED MODULATION

As the schematic shown in Fig. 2, the BSRC consists of a primary full-bridge circuit and a secondary full-bridge circuit, interconnected with a series resonant tank ($L_r$ – $C_r$) and a transformer. MOSFET switches $S_1$ to $S_8$ in the primary full-bridge circuit are modulated to generate AC voltage $v_{ab}$ from the primary DC bus $V_1$. The transformer provides voltage isolation and step-down with a turn ratio of $n : 1$. The secondary full-bridge circuit includes MOSFET switches $S_5$ to $S_8$, which are modulated to generate AC voltage $v_{cd}$ from the secondary DC bus $V_2$. The magnetic inductance is large enough and the series resonant tank is considered to be insusceptible.

The proposed modulation can be divided into 8 working modes, where 4 are for the forward power flow and 4 are for the reverse power flow. The forward power flow includes Mode 1 (boost operation), Mode 2 (buck operation at high power level), Mode 3 (buck operation at medium power level), and Mode 4 (buck operation at low power level). Likewise, the reverse power flow includes Mode 5 (boost operation), Mode 6 (buck operation at high power level), Mode 7 (buck operation at medium power level), and Mode 8 (buck operation at low power level). Due to the symmetric topology of the series resonant tank, the switching patterns and waveforms are identical for the forward and reverse modes, and thus only the analysis of the forward modes, i.e., Mode 1–4, will be given in Section II. It should be noted that Modes 5–8 are dual to Mode 1–4, and thus they will not be repeated.

A. Summarized Operating States

In a half switching cycle, according to the ON/OFF states of the switches $S_1$ to $S_8$, six possible operating states are firstly identified and summarized in Table II. An illustration is also given as follows.

1) State A: $S_1$ and $S_4$ are ON, while $D_5$ and $D_8$ are conducting. $i_r$ flows through the resonant tank in the forward direction. The power is fed from $V_1$ to $V_2$.

2) State B: $S_2$ and $S_4$ are ON, while $D_6$ and $D_7$ are conducting. $i_r$ flows through the resonant tank in the reverse direction. The power is released from the resonant tank to $V_2$.

3) State C: $S_2$ and $S_4$ are ON, while $D_5$ and $D_8$ are conducting. $i_r$ flows through the resonant tank in the forward direction. The power is released from the resonant tank to $V_2$.

4) State D: $S_1$, $S_4$, $S_6$, and $S_8$ are ON. $i_r$ flows through the resonant tank in the forward direction. The power is released from $V_1$ to the resonant tank.

5) State N1 and N2: $S_3$ to $S_8$ are OFF. The secondary terminal of the resonant tank is open, and there is no power flow.

It can be found that the instantaneous power, flowing from the output side to the input side during the whole switching period, is nonnegative, no matter whether the state is A–D, N1 or N2. Therefore, any combination of these states can provide non-backflow-power features. In order to simplify the analysis of each working mode, all variables in the following are normalized with the base values of voltage and impedance being:

$$V_{\text{base}} = V_1$$

$$Z_{\text{basic}} = Z_r = \sqrt{\frac{L_r}{C_r}}$$

and

$$\omega_r = \frac{1}{\sqrt{L_r C_r}}$$

respectively. Therefore, $M = (nV_2/V_1)$, $j_r = (i_r Z_r/V_1)$, and $m_r = (v_r/V_1)$ are defined as the normalized output voltage, resonant current and resonant voltage, respectively. $\omega_r t$ is represented by $\varphi$. And $j_{r,1}$ and $m_{r,1}$ are the instantaneous values of $j_r$ and $m_r$ at $\varphi_1 = \omega_r t_1$. 

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Fig. 2. Schematics of a BSRC.
TABLE II
SUMMARIZED OPERATING STATES OF THE BSRC

<table>
<thead>
<tr>
<th>Switches ON/OFF</th>
<th>Equivalent circuit</th>
<th>Power drawing</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>State A</td>
<td><img src="image1" alt="State A Circuit" /></td>
<td><img src="image2" alt="State A Power" /></td>
<td>Power transduction</td>
</tr>
<tr>
<td>State B</td>
<td><img src="image3" alt="State B Circuit" /></td>
<td><img src="image4" alt="State B Power" /></td>
<td>Power release</td>
</tr>
<tr>
<td>State C</td>
<td><img src="image5" alt="State C Circuit" /></td>
<td><img src="image6" alt="State C Power" /></td>
<td>Power release</td>
</tr>
<tr>
<td>State D</td>
<td><img src="image7" alt="State D Circuit" /></td>
<td><img src="image8" alt="State D Power" /></td>
<td>Power storage</td>
</tr>
<tr>
<td>State N1</td>
<td><img src="image9" alt="State N1 Circuit" /></td>
<td><img src="image10" alt="State N1 Power" /></td>
<td>Power block</td>
</tr>
<tr>
<td>State N2</td>
<td><img src="image11" alt="State N2 Circuit" /></td>
<td><img src="image12" alt="State N2 Power" /></td>
<td>Power block</td>
</tr>
</tbody>
</table>

B. Mode 1: Boost Operation

Fig. 3 shows the switching patterns and the operating waveforms of Mode 1. There exist three stages as follows.

1) Stage 1 (0 ≤ ϕ < ϕ₁) (State D): The cycle starts with zero resonant current iᵣ at ϕ = 0, and thus S₁, S₄, S₆, and S₈ achieve ZCS-ON. v₊ib is connected with V₁ and v₋cd is shorted by S₆ and S₈, such that the power is stored in the resonant tank. iᵣ will increase sinusoidally, and the state equations are given by

\[ jᵣ = (1 - mᵣ₁ - M) \sin (ϕ - ϕ₁) + jᵢ₁ \sin (ϕ - ϕ₁) \]
\[ mᵣ = -(1 - mᵣ₁ - M) \cos (ϕ - ϕ₁) + 1 - M. \]

2) Stage 2 (ϕ₁ ≤ ϕ < ϕ₂) (State A): S₁ and S₄ are kept ON. D₅ and D₈ conduct when S₆ and S₈ are turned off at ϕ₁, which is determined by the duty cycle of secondary side D₅, donated by ϕ₁ = 2πDₛ. The power is delivered from V₁ to V₂, and the state equations can be derived as follow:

\[ jᵣ = (1 - mᵣ₁ - M) \sin (ϕ - ϕ₁) + jᵢ₁ \sin (ϕ - ϕ₁) \]
\[ mᵣ = -(1 - mᵣ₁ - M) \cos (ϕ - ϕ₁) + 1 - M. \]

3) Stage 3 (ϕ₂ ≤ ϕ < π) (State N1): jᵣ keeps zero and mᵣ maintains mᵣ₂ during this period since the converter is open-circuit, which could be valid only if mᵣ₂ ≤ 1 + M.

In Mode 1, the operation is similar to the discontinuous current mode (DCM) of a boost converter. In Stage 1, power is stored in the resonant tank like ON-state of the boost converter. In Stage 2, power is delivered from V₁ and the resonant tank to V₂ like the OFF-state of the boost converter. In Stage 3, power is blocked like the OFF-state of the boost converter. Similarly, Dₛ can be adjustable for power regulation. Dₚ is fixed to 0.5, and the operating frequency fₛ is fixed at the resonant frequency.
There is no backflow power between the two voltage sources in this mode. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle in this mode.

C. Mode 2: Buck Operation at High Power Level

Fig. 4 shows the switching patterns and operating waveforms of the buck operation at a high power level. There exist two operating stages as follows.

1) Stage 1 ($0 \leq \phi < \phi_1$) (State A): $S_4$, $D_5$, and $D_8$ are kept ON. At $\phi = 0$, $S_1$ is turned ON. $i_r$ increases sinusoidally with time to deliver power from the primary to the secondary, and it can be derived as follow:

$$j_r = (1 - m_{r0} - M) \sin \phi + j_{r0} \cos \phi$$

$$m_r = (-1 + m_{r0} + M) \cos \phi + j_{r0} \sin \phi + 1 - M.$$  

2) Stage 2 ($\phi_1 \leq \phi < \phi_2$) (State B): At $\phi_1$, the resonant current $i_r$ reaches zero, such that $S_1$, $D_3$, and $D_4$ are ZCS-OFF, while $S_2$, $D_6$, and $D_7$ are ZCS-ON. During this stage, $i_r$ is negative and still charges $V_2$ to release the power stored in the resonant tank. $\phi_2$ is $\pi f_r / f_s$, equals a half of the switching period, when $S_4$ turns OFF with negative current realizing ZVS-OFF. The state equations can be derived as follow:

$$j_r = (M - m_{r1}) \sin (\phi - \phi_1)$$

$$m_r = (m_{r1} - M) \cos (\phi - \phi_1) + M.$$  

In Mode 2, the operation is similar to a buck converter. In Stage 1, power is delivered from $V_1$ to $V_2$ like the ON-state of the buck converter. In Stage 2, the power is released from the resonant tank to $V_2$ like the OFF-state of the buck converter. The switching frequency $f_s$ can be adjusted to control the amount of power delivery, like the constant-ON time control of the buck converter. The lower $f_s$, the smaller amount of power is delivered. $f_s$ ranges from $f_r$ to $(f_r/2)$, i.e., $f_r/2 \leq f_s \leq f_r$ in this operation. There is no backflow power, thus decreasing the resonant current. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle in this mode.

D. Mode 3: Buck Operation at Medium Power Level

The delivered power decreases with the decrease of the switching frequency. When the switching frequency is smaller than half of the resonant frequency, i.e., $f_r < (f_r/2)$, the converter operates at Mode 3. Fig. 5 shows the switching patterns and operating waveforms. There exists three operation stages as follows.

1) Stage 1 ($0 \leq \phi < \pi$) (State A): At $\phi = 0$, $i_r$ rises from zero, and thus $S_1$, $D_3$, and $D_4$ are ZCS-ON. $S_4$ is kept ON. This mode ends when $i_r$ reaches zero again at $\phi = \pi$, which is about half of the resonant period. The state equations can be derived as follow:

$$j_r = (1 - m_{r0} - M) \sin \phi$$

$$m_r = (-1 + m_{r0} + M) \cos \phi + j_{r0} \sin \phi + 1 - M.$$  

Fig. 5. Switching patterns and operating waveforms of Mode 3.
be derived as follow:
\[ j_r = (1 - m_{r_0} - M) \sin \varphi \] (16)
\[ m_r = (-1 + m_{r_0} + M) \cos \varphi + 1 - M. \] (17)

2) Stage 2 (\( \varphi_1 \leq \varphi < \varphi_2 \)) (State C): At \( \varphi_1 \), \( S_1 \) is turned off. \( i_r \) flows through \( D_2 \), making \( S_2 \) ZVS-ON. The power stored in the resonant tank is released to \( V_2 \). The state equations can be derived as follow:
\[ j_r = (-M - m_{r_1}) \sin (\varphi - \varphi_1) + j_{r_1} \cos (\varphi - \varphi_1) \] (18)
\[ m_r = (m_{r_1} + M) \cos (\varphi - \varphi_1) + j_{r_1} \sin (\varphi - \varphi_1) - M. \] (19)

3) Stage 3 (\( \varphi_2 \leq \varphi < \varphi_3 \)) (State B): At \( \varphi_2 \), \( i_r \) reaches zero again. Thus, \( D_5 \) and \( D_8 \) are ZCS-OFF. The state equations can be derived as follow:
\[ j_r = (M - m_{r_2}) \sin (\varphi - \varphi_2) \] (20)
\[ m_r = (m_{r_2} - M) \cos (\varphi - \varphi_2) + M. \] (21)
i_r charges \( V_2 \) to release the power stored in the resonant tank. And this period could work for half resonant cycle.

4) Stage 4 (\( \varphi_3 \leq \varphi < \varphi_4 \)) (State N2): \( i_r \) is discontinuous from \( \varphi_3 \) to \( \varphi_4 \). \( D_6 \) and \( D_7 \) are ZCS-OFF. The output circuit stops working. \( i_r \) remains null until the next half cycle, which could occur only if \( m_{r_3} \geq -M \).

The Mode 4 is also similar to the DCM of a buck converter. Stage 1 is like the ON-state, Stage 2 and Stage 3 are like the OFF-state with circulating current, and Stage 4 is like the OFF-state without circulating current. Since \( f_s \) is fixed to \( f_{m_{\text{min}}} \), \( D_p \) is regulated to control the delivered power. Smaller \( D_p \) contributes to lowering the delivered power. There is no backflow power in this mode. Seven of eight (7/8) switching actions are soft switching during half of the switching cycle.

III. OUTPUT CHARACTERISTIC AND CONTROL SCHEME

A. Analysis of Output Characteristic

Based on the modulation scheme proposed in Section II, the control variables for the four working modes (forward power flow as an example) are not identical. In Mode 1, \( D_S \) is controlled for output power regulation. \( f_s \) is responsible for Modes 2 and 3, while \( D_p \) takes charge of Mode 4.

With the state equations derived in Section II, an accurate model can be built for the BSRC to analyze the output characteristic. It is noteworthy that, it is difficult to get analytical solutions to these nonlinear equations, and alternatively a numerical way with the help of MATLAB is used in this article [34]. The boundary conditions are highlighted in Appendix. Table III summarizes the corresponding control variables as well as their range for each working mode. The curves of output power versus control variables for different working modes are depicted in Fig. 7 and illustrated as follows.

1) Mode 1: The switching frequency is fixed as \( f_s = f_r \), while the conducting time \( D_{pT} \) of \( S_0 \) and \( S_8 \) is controlled to regulate the output power. Curves plotted in Fig. 7(a) show the normalized delivered power versus the duty cycle \( D_p \) under different voltage gain \( M \). As shown in Table III, \( D_p \) varies from 0 to \( D_p_{\text{max}} \) to regulate the output power ranging from 0 to \( P_{\text{max}} \), which is the maximum power calculated in...
TABLE III
CONTROL VARIABLE AND ITS RANGE FOR EACH WORKING MODE

<table>
<thead>
<tr>
<th>Working Mode</th>
<th>( f_s )</th>
<th>( D_p )</th>
<th>( D_s )</th>
<th>( P )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode 1</td>
<td>( f_r )</td>
<td>0.5</td>
<td>( [0, D_{s,\text{max}}] )</td>
<td>( [0, P_{1,\text{max}}] )</td>
</tr>
<tr>
<td>Mode 2</td>
<td>([0.5 f_r, f_r])</td>
<td>0.25, 0.5</td>
<td>0</td>
<td>( [P_1, +\infty) )</td>
</tr>
<tr>
<td>Mode 3</td>
<td>([f_{\min}, 0.5 f_r])</td>
<td>([f_{\min}, 0.25])</td>
<td>0</td>
<td>( [P_2, P_3] )</td>
</tr>
<tr>
<td>Mode 4</td>
<td>( f_{\min} )</td>
<td>([0, f_{\min}/f_r])</td>
<td>0</td>
<td>( [0, P_2] )</td>
</tr>
</tbody>
</table>

1) \( p_1 \) = \( \frac{n V_1 V_2}{n V_1 V_2} \), \( p_2 \) = \( \frac{2 n V_1 V_2}{n V_1 V_2} \).

Fig. 7. Normalized power against the duty cycle and switching frequency with the proposed modulation scheme. (a) Boost operation (Mode 1). (b) Buck operation (Mode 2–4).

Section IV-B. The delivered power increases with the increase of \( D_s \).

2) Mode 2: \( D_s \) is fixed at 0, and \( f_s \) is controlled to regulate the output power. \( D_p \) is determined by \( f_s \) according to (A.15). Curves plotted in Fig. 7(b) show the normalized delivered power versus the switching frequency \( f_s \) under different voltage gain \( M \). As shown in Table III, \( f_s \) varies from 0.5\( f_r \) to \( f_r \) to regulate the output power ranging from \( P_1 \) to infinity. Correspondingly, \( D_p \) varies from 0.25 to 0.5. The delivered power increases with the increase of \( f_s \).

3) Mode 3: \( D_s \) is fixed at 0, and \( f_s \) is controlled to regulate the output power. Unlike that in Mode 2, \( D_p \) is determined by \( f_s \) according to (A.20). Curves plotted in Fig. 7(b) show the normalized delivered power versus the switching frequency \( f_s \) under different voltage gain \( M \). As shown in Table III, \( f_s \) varies from \( f_{\min} \) to 0.5\( f_r \) to regulate the output power ranging from \( P_2 \) to \( P_1 \). Correspondingly, \( D_p \) varies from \( (f_{\min}/2 f_r) \) to 0.25. The delivered power increases with the increase of \( f_s \).

4) Mode 4: \( D_s \) and \( f_s \) are fixed at 0 and \( f_{\min} \), respectively. \( D_p \) is controlled to regulate the output power. Curves plotted in Fig. 7(b) show the normalized delivered power versus the duty cycle \( D_p \) under different voltage gain \( M \). As shown in Table III, \( D_p \) varies from 0 to \( (f_{\min}/2 f_r) \) to regulate the output power ranging from 0 to \( P_2 \). The delivered power increases with the increase of \( D_p \).

It can be observed from Table III and Fig. 7 that, the control variables, \( D_s \), \( D_p \), and \( f_s \), can continuously vary to regulate the delivered power among different working modes.

B. Control Scheme

Based on the analysis in Section III-A, each working mode has an identical modulation scheme and output characteristic. The controller design first begins with power regulation in each working mode, as shown in Fig. 8. In this case, \( V_2 \) is controlled to track \( V_{2\text{ref}} \) for forward and reverse power flow conditions. Similarly, \( V_1 \) also can be regulated to track \( V_{1\text{ref}} \).

1) In Mode 1, \( f_s \) and \( D_p \) are fixed at \( f_r \) and 0.5, respectively. \( D_s \) is controlled for power regulation.
2) In Mode 2, \( f_s \) is regulated to control the power, and \( D_p \) is correlatively determined by \( f_s \) based on (A.15). \( D_s \) keeps zero.
3) In Mode 3, \( f_s \) is kept controlled, and \( D_p \) is correlatively determined by \( f_s \) according to (A.20).
4) In Mode 4, \( D_p \) is regulated to control the power with a fixed minimum switching frequency \( f_{\min} \).

Moreover, since the output power has a monotonic relationship with the corresponding control variable in all the working modes, simple PI controllers can be used.

Then, the seamless switchover between the working modes is based on a state flowchart, as shown in Fig. 9. \( P \) is defined as positive when the power is delivered from \( V_1 \) to \( n V_2 \). The initial state is determined by the output voltage \( V_2 \), the desired output voltage value \( V_{2\text{ref}} \) and voltage gain \( M = n V_2/V_1 \). The criteria are given as follows.

1) If \( M \leq 1 \) and \( V_{2\text{ref}} \geq V_2 \), converter enters into Mode 2.
2) If \( M \leq 1 \) and \( V_{2\text{ref}} < V_2 \), converter enters into Mode 5.
3) If \( M > 1 \) and \( V_{2\text{ref}} \geq V_2 \), converter enters into Mode 1.
4) If \( M > 1 \) and \( V_{2\text{ref}} < V_2 \), converter enters into Mode 6.

The rest operating principle of the state flowchart can be detailed as follows.

1) In Mode 1, if \( D_s \leq 0 \) and \( V_2 > V_{2\text{ref}} \) & \( P > 0 \), the BSRC jumps to Mode 2 through path (1). However, if \( V_2 < V_{2\text{ref}} \) & \( D_s \leq 0 \) & \( P < 0 \), the BSRC reverses the power flow direction and jumps to Mode 8 via path (9). Unless specified otherwise.
2) In Mode 2, when \( f_s \leq f_r/2 \), the BSRC jumps to Mode 3 through path (2). But if \( f_s \geq f_r/2 \) & \( V_2 < V_{2\text{ref}} \), the BSRC jumps back to Mode 1 through path (6).
3) In Mode 3, when \( f_s \) is below \( f_{\min} \), the BSRC jumps to Mode 4 through path (3). But if \( f_s \) is above \( f_r/2 \), the BSRC jumps back to Mode 2 via path (5).
4) In Mode 4, when \( V_2 > V_{2\text{ref}} \) & \( D_p \leq 0 \) & \( P \leq 0 \), the BSRC reverses the power flow direction and works at Mode 5 via path (4). But if the duty cycle \( D_p \) is...
increased to be above $f_{\text{min}}/2 f_c$ for more output power, the BSRC jumps back to Mode 3 through path (3).

In order to make the control variables seamless transfer among different working modes, when the converter enters a new working mode, it is not necessary to start the controller from an initialized state. The initial values of the controllers in the “ready-to-go” working modes will also be updated with the controller in the currently “in-use” working mode. Thus the output power, switching frequency, and duty cycle are continuously regulated.

### IV. RMS Resonant Current and Soft Switching

#### A. RMS Resonant Current

In order to evaluate the rms resonant current of the proposed modulation method, the rms value of $i_r$ in the article is compared between different modulations since the conduction loss is only associated with the rms current in the switches and the transformer. Then the normalized rms value of $i_r$ is represented as follows:

$$j_{r, \text{rms}} = \frac{i_{r, \text{rms}}}{I_1}$$

where $I_1$ is the input current that can be calculated by

$$I_1 = \begin{cases} \frac{2}{T_s} \int_{t_0}^{t_1} i_c \, dt, & \text{for Mode 1} \\ \frac{2}{T_s} \int_{t_0}^{t_1} i_c \, dt, & \text{for Mode 2~4} \end{cases}$$

$i_{r, \text{rms}}$ is the rms value of resonant current. $j_{r, \text{rms}}$ can represent the conduction loss of the converter for delivering the same power. Larger $j_{r, \text{rms}}$ means larger conduction losses.

In order to verify the proposed method, the analytical and simulated rms resonant current curves with respect to the delivered power for different voltage gain are plotted in Fig. 10. As the figure shows, the normalized rms values could decrease with respect to the increase of the delivered power. And when the voltage gain is close to 1, the normalized rms value could fall. The normalized rms value of the proposed modulation is observably lower than the other two modulations, PSM and VFM + PSM. This means the conduction losses of the proposed modulation can be reduced due to non-backflow-power. The same conclusion is also given in [30] and [31]. In particular, $D_5$–$D_8$ are uncontrolled rectification in the proposed modulation. However, $S_5$–$S_8$ for VFM + PSM method realize synchronous rectification (SR) resulting in small conduction loss. When SR is implemented in the proposed modulation, the conduction loss can be further reduced as well.

#### B. Critical Conditions for Soft Switching

Critical conditions for soft switching among all the working modes (forward power flow as an example) are analyzed as follows.
Fig. 10. Curves of normalized rms resonant current versus delivered power with different modulations. (a) Proposed, (b) PSM, and (c) VFM + PSM modulation.

1) Mode 1: Based on the operating principle of Mode 1 illustrated in Section II-B, $i_r$ should be positive at $\varphi_1$, while it should keep zero during $\varphi_2 \sim \pi$. Thus, the critical condition of soft switching in Mode 1 can be derived as follow:

$$m_{r2} < 1 + M$$  \hspace{1cm} (24)

and

$$j_{r1} \geq 0.$$  \hspace{1cm} (25)

With the mode solver demonstrated in Appendix, Fig. 11 plots the normalized output current $J_o$ versus the normalized output voltage $M$ when $m_{r2} = 1 + M$. To satisfy (24), the BSRC should operate in the area below the curve. The maximum normalized output current can be readily achieved from the curve, donated by $J_{o,max}$. Within the operating region, the delivered power should not be over $P_{max} = J_{o,max} M V_1^2/Z_r$.

With (A.1), $j_{r1}$ can be rewritten as follow:

$$j_{r1} = (1 - m_{r0}) \sin \varphi_1$$  \hspace{1cm} (26)

where $0 \leq \varphi_1 < \pi$. Thus $\sin \varphi_1 \geq 0$. Since the peak value of resonant voltage $|m_{r0}|$ increase with power, $m_{r0} = 0$ is the maximum value at $D_s = 0$, when $|m_{r0}|$ reaches the minimum value. Such that, $1 - m_{r0} \geq 1$, and (25) can be always satisfied in Mode 1.

In brief, when $P \leq P_{max}$, the BSRC can realize soft switching in Mode 1.

2) Mode 2: Based on the operating principle of Mode 2 illustrated in Section II-C, $i_r$ should keep zero at $\varphi_1$, while it should be positive at $0$. Thus, the critical condition of soft switching at Mode 2 can be derived as follow:

$$j_{r1} = 0$$  \hspace{1cm} (27)

and

$$|j_{r0}| > 0.$$  \hspace{1cm} (28)

Equation (27) is the constrain condition for Mode 2, as given in (A.6). The duty cycle $D_p$ complies with (A.15) to satisfy (27). With (A.12), $j_{r0}$ can be rewritten as follow:

$$|j_{r0}| = -\sin \varphi_1 \sin (\varphi_2 - \varphi_1).$$  \hspace{1cm} (29)

Since $j_{r2} = -j_{r0}$ and $\pi \leq \varphi_2 \leq 2\pi$ for $f_r \geq f_s \geq 0.5f_r$, there only exists a zero-cross point $\varphi_1$ during $0$ to $\varphi_2$. Then $0 < \varphi_1 < \pi$, and $0 < (\varphi_2 - \varphi_1) < \pi$. Such that, (28) can always be satisfied in Mode 2.

In brief, if $D_p$ complies with (A.15), the BSRC can achieve soft switching in Mode 2 without sensing $i_r$.

3) Mode 3: Based on the operating principle of Mode 3 illustrated in Section II-D, $i_r$ should be zero at $0$, $\varphi_1$ and $\varphi_2$. Since $\varphi_1$ and $\varphi_2$ are the half and one resonant cycle, respectively, only if $i_r$ is zero at $0$, the BSRC can realize soft switching. Thus $i_r$ should be discontinuous, and the critical condition of soft switching in Mode 3 can be derived as follow:

$$m_{r2} \geq -M.$$  \hspace{1cm} (30)

Based on (A.19), $m_{r2}$ can be rewritten as follow:

$$m_{r2} = 2M - 1.$$  \hspace{1cm} (31)

Fig. 11. Boundary of soft switching in Mode 1.
Thus, when the following inequality is satisfied, the BSRC can achieve soft switching in Mode 3

\[ \frac{1}{3} \leq M \leq 1. \]  

(32)

4) Mode 4: Based on the operating principle of Mode 4 illustrated in Section II-E, \( i_r \) is zero at 0, \( \phi_2 \) and \( \phi_3 \). Due to the natural commutation, \( i_{r2} = 0 \) and \( i_{r3} = 0 \) can be obtained. To satisfy \( i_{0} = 0 \), \( i_0 \) should be discontinuous. Meanwhile, ZVS-ON of \( S_2, S_4 \) can be achieved only when \( i_r > 0 \) at \( \phi_1 \). Thus, the critical condition of soft switching in Mode 4 can be derived as follow:

\[ m_{r3} \geq -M \]  

(33)

and

\[ j_{r1} > 0. \]  

(34)

Since \( m_{r3} \) decreases with the increase of delivered power, the minimum value of \( m_{r3} \) in Mode 4 is \( 2M - 1 \), when \( D_p = (f_{\text{min}}/2f_r) \). To satisfy (33), \( M > (1/3) \) should be satisfied. With (A.21), the minimum value of \( j_{r1} \) can be written as follow:

\[ j_{r1,\text{min}} = (1 + m_{r3,\text{min}} - M) \sin \phi_1 = M \sin \phi_1. \]  

(35)

Thus, (34) can always be satisfied.

In brief, if \( (1/3) \leq M \leq 1 \), the BSRC can achieve soft switching in Mode 4.

In conclusion, based on the analysis of critical conditions for soft switching in the four working modes, the intersected critical conditions for soft switching can be highlighted as follow:

\[ P \leq P_{\text{max}}, \quad \text{for Mode 1} \]  

(36)

\[ M \geq \frac{1}{3}, \quad \text{for Mode 2, 3, and 4}. \]  

(37)

Once (36) and (37) are both satisfied via the design of resonant tank \( Z_r \) and transformer \( n \), soft switching can be achieved for the wide operating range.

C. Summary of Switching Loss

The switching features for the proposed modulation are summarized in Table IV. In general, there are 8 switches in the BSRC, and thus each switching cycle includes 16 switching actions. For the conventional VFM + PSM [18], although 8 turn-on actions realize soft switching, the other 8 turn-off actions suffer from hard switching that cannot be ignored especially when there exists large turn-off current. It can be observed that 14 of the total 16 switching actions are soft-switching in Mode 1, Mode 2, and Mode 4. Moreover, all switching actions are soft switching in Mode 3. Due to the switch capacitance, there is still ZCS-OFF loss, which is given as follows:

\[ P_{\text{ZCS-OFF}} = \frac{1}{2}C_{ds}V_{dc}^2. \]  

(38)

\( V_{dc} \) is the DC voltage and \( C_{ds} \) is the drain–source capacitance of the switches.

| TABLE IV |
| SOFT SWITCHING FEATURES OF THE PROPOSED MODULATION SCHEME |

<table>
<thead>
<tr>
<th>Boost mode</th>
<th>Mode 1</th>
<th>Mode 2</th>
<th>Mode 3</th>
<th>Mode 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>( S_1 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>ZCS</td>
<td>Non-ZCS</td>
</tr>
<tr>
<td>( S_2 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_3 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>Non-ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_4 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_5 )</td>
<td>Turn on</td>
<td>ZVS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_6 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_7 )</td>
<td>Turn on</td>
<td>ZVS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>( S_8 )</td>
<td>Turn on</td>
<td>ZCS</td>
<td>ZCS</td>
<td>ZCS</td>
</tr>
<tr>
<td>Soft switching</td>
<td>14/16</td>
<td>14/16</td>
<td>16/16</td>
<td>14/16</td>
</tr>
</tbody>
</table>

For the conventional methods with single ZVS-ON and hard-OFF, the ZVS-ON loss is eliminated but large hard-OFF loss appears, which is

\[ P_{\text{hard OFF}} = \frac{1}{2}V_{dc}i_{\text{OFF}}f_\text{OFF}. \]  

(39)

where \( i_{\text{OFF}} \) is the turn-off current and \( f_\text{OFF} \) is the switching falling time. As the analysis in Section I, \( f_\text{OFF} \) could be very large, especially in light load conditions. Thus the total switching loss could be very large in the modulations with single ZVS-ON and hard-OFF. The comparison between the conventional methods with single ZVS-ON and hard-OFF and ZCS-ON/OFF method has also given in [38], which verified that the ZCS-ON/OFF has efficiency advantages over conventional sole ZVS-ON and hard-OFF.

Therefore, in the first place, the proposed modulation cures the problem of hard turn-off loss by reducing the number of hard switching actions. In the second place, with the proposed modulation, the magnitude of the turn-off current is significantly reduced compared with the conventional VFM + PSM, as shown in Fig. 12. Such that, the problem of the turn-off loss can be further alleviated.

V. EXPERIMENTAL VERIFICATION

As shown in Fig. 13, a 1 kVA experimental prototype of the BSRC is built with specifications and parameters given in Table V. The magnetic devices are designed according to \( 0.5f_r = 100 \) kHz. Because when magnetic current \( i_m \) is zero, the magnetic flux density \( B \) could be fixed, and no magnetic loss could appear. In the proposed modulation, the longest conduction time of resonant current \( i_r \) is \( 2T_r \) for all the operation modes as shown in Figs. 3–6, \( i_r \) is zero during other times, as well as magnetic current. The minimum varying frequency of \( i_m \) is \( 0.5f_r \).

A. Measured Operating Waveforms

Typical operating waveforms of the BSRC in the forward mode and the reverse mode are shown in Figs. 14 and 15,
Figs. 12. Turning current of proposed modulation versus VFM + PSM modulation. (a) $M = 2.5$ in the boost operation (Mode 1). (b) $M = 0.4$ in the Buck operation (Mode 2–4).

TABLE V

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Symbols</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary side</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage range</td>
<td>$V_1$</td>
<td>240 – 480 V</td>
</tr>
<tr>
<td>Nominal voltage</td>
<td>$V_{1,nom}$</td>
<td>400 V</td>
</tr>
<tr>
<td>Current range</td>
<td>$I_1$</td>
<td>0 – 2.5 A</td>
</tr>
<tr>
<td>Secondary side</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage range</td>
<td>$V_2$</td>
<td>24 – 56 V</td>
</tr>
<tr>
<td>Nominal voltage</td>
<td>$V_{2,nom}$</td>
<td>48 V</td>
</tr>
<tr>
<td>Current range</td>
<td>$I_2$</td>
<td>0 – 20 A</td>
</tr>
<tr>
<td>Parameters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Primary-side switches</td>
<td>$S_1 - S_4$</td>
<td>E3M0065090D</td>
</tr>
<tr>
<td>Secondary-side switches</td>
<td>$S_5 - S_8$</td>
<td>E3MIP0030N10NSD</td>
</tr>
<tr>
<td>Resonant inductor</td>
<td>$L_r$</td>
<td>50 µH</td>
</tr>
<tr>
<td>Resonant capacitor</td>
<td>$C_r$</td>
<td>12 nF</td>
</tr>
<tr>
<td>Resonant frequency</td>
<td>$f_r$</td>
<td>200 kHz</td>
</tr>
<tr>
<td>Turn ratio</td>
<td>$n$</td>
<td>16:2</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_s$</td>
<td>50 – 200 kHz</td>
</tr>
</tbody>
</table>

respectively. Since the forward mode and the reverse mode are symmetric, only an illustration of the operating waveforms in the forward mode is performed as follows.

For Modes 2–4, the normalized gain $M$ is 0.4 with the input voltage being 480 V and the output voltage being 24 V. In Mode 2, the switching frequency is about 110 kHz which is between the resonant frequency 200 kHz and half of the resonant frequency 100 kHz. As shown in Fig. 14(a), $S_2$ and $S_1$ are turned OFF when $i_r$ flows through the anti-parallel diodes, and turned ON when $i_r = 0$, thus realizing zero loss switching. As the complements of $S_2$ and $S_4$, $S_1$ and $S_3$ realize ZCS-OFF but suffer from hard turn-on. $S_5$–$S_8$ operate at rectification mode, realizing ZCS-ON and OFF. In Mode 3, $f_s$ is about 71 kHz below half of the resonant frequency. As shown in Fig. 14(b), all the switches turn ON/OFF when $i_r = 0$, thus realizing ZCS-ON/OFF. In Mode 4, $f_s$ is fixed to
50 kHz, and $D_p$ is controlled to regulate the power. As shown in Fig. 14(c), $S_2$ and $S_4$ realize ZVS-ON and ZCS-OFF. $S_1$ and $S_3$ are complements of $S_2$ and $S_4$, thus realizing ZCS-ON but suffering from hard turn-off.

For Mode 1, the normalized gain $M$ is 1.87 with the input voltage being 240 V and the output voltage being 56 V. As shown in Fig. 14(d), $f_s$ is 200 kHz, and $D_a$ is regulated to control the power. $S_1$ and $S_3$ are complements of $S_2$ and $S_4$, and $S_2$ is synchronous with $S_3$. The switches $S_1$–$S_4$ are controlled in complementary at duty 50% and turn ON/OFF with zero current. Output full-bridge operates at rectification mode. $S_6$ and $S_8$ are ZCS-ON.

In summary, 14 of the total 16 switching actions are soft-switching in Modes 1, 2, and 4, while all switching actions are soft switching in Mode 3. The reduction of the number of hard switching actions can help to reduce the switching losses, which will be verified in Section V-D.

In the reverse mode, the waveforms are similar to those of the forward mode, as shown in Fig. 15. The switching patterns, operating waveforms, and features of the switching actions are consistent with the analysis in Section II.

### B. Mode Transition Waveforms

Fig. 16(a) shows the transition from Mode 4 (buck mode with low power level) to Mode 3 (buck mode with medium power level). The input voltage is 400 V, and the output voltage is regulated to 40 V. At the beginning, the load resistor is 7.5 $\Omega$. The turning ON time is set to 1.69 $\mu$s, the converter works in Mode 4. Then the load is changed to 5 $\Omega$. Mode 4 is switched to Mode 3, and the turning ON time rises from 1.69 to 2.32 $\mu$s, then the switching frequency is regulated from 50 to 55 kHz. Similarly, the transition from Mode 3 to Mode 4 is given in Fig. 16(b) with the same condition. The load is changed from 7.5 to 5 $\Omega$. The operation mode can be seamlessly switched between Mode 4 and Mode 3.

Fig. 16(c) shows the transition from Mode 3 to Mode 2 (buck mode with high power level). The input voltage is 400 V, and the output voltage is regulated to 40 V. At the beginning, the load resistor is 4 $\Omega$. The turning ON time is set to 2.32 $\mu$s, the converter works in Mode 3. Then the load is changed to 2.5 $\Omega$. Mode 3 is switched to Mode 2, and the switching frequency is regulated from 66 to 110 kHz. Then Fig. 16(d) shows the transition from Mode 2 to Mode 3 under the same condition. The load is changed from 4 to 2.5 $\Omega$. The transition waveforms verify that the operation mode can be seamlessly switched between Mode 3 and Mode 2.

Fig. 16(e) shows the transition between Mode 2 and 1 (boost mode). Because the boundary between buck and boost modes is the voltage gain $M = 1$. Thus the output voltage must be changed to realize the transition between buck and boost mode. The input voltage is 400 V, the output load is 5 $\Omega$. In the beginning, the output voltage is 48 V and the converter works in Mode 2. Then Mode 2 is switched to Mode 1, and thus the switching frequency continues to rise from 126 to 200 kHz, then the conduction time $D_s T_s$ of $S_8$ is continuously increased from 0 to 0.348 $\mu$s, until the output reaches a steady state. Similarly, the transition from Mode 1 to Mode 2 is given in Fig. 16(f) with the same condition. The output voltage is regulated from 56 to 48 V, showing the operation mode can be seamlessly switched between Mode 2 and Mode 1.

Fig. 16(g) shows the transition between Mode 1 and 8 (buck mode with low power level for reverse power). The input voltage is 400 V, and the output voltage is controlled to be 56 V. In the beginning, the output load current is 10 A and the converter works in Mode 1. Then the output load is reversed to be −4 A. The the conduction time $D_s T_s$ of $S_8$ is continuously decreased from 0.404 $\mu$s to 0. Then the converter works into Mode 8 and the switching frequency is switched to 50 kHz. Similarly, the transition from Mode 8 to Mode 1 is given in Fig. 16(h) with the same condition. The output load current is changed from −4 to 10 A. The operation mode can be seamlessly switched between Mode 1 and Mode 8.

Seamless transitions among different working modes can be achieved. Moreover, the computation time is only 5 $\mu$s.
Fig. 16. Transitions waveforms between different work modes. Transition from (a) Mode 4 to 3, (b) Mode 3 to 4, (c) Mode 3 to 2, (d) Mode 2 to 3, (e) Mode 2 to 1, (f) Mode 1 to 2, (g) Mode 1 to 8, and (h) Mode 8 to 1.

to update the switching sequence. The settling time is about 10 ms, which is acceptable compared with other papers.

C. Measured Circulation Current

With the direct measurement of the input current $I_1$ and the rms value of $i_r$, the normalized rms resonant current can be obtained through the calculation with (22). Fig. 17 shows the measured rms resonant current $j_{r,rms}$ for the proposed modulation and the conventional VFM + PSM, under different input and output settings. Solid curves represent $j_{r,rms}$ for the proposed modulation, while dashed curves represent that for the VFM + PSM. In Fig. 17(a), the BSRC is in the forward
Fig. 17. Measured normalized rms resonant current versus output power.
(a) Forward mode with $V_2 = 48$ V. (b) Reverse mode with $V_1 = 400$ V.

Fig. 18. Measured efficiency versus power. (a) Forward mode with $V_2 = 48$ V. (b) Reverse mode with $V_1 = 400$ V.

mode. The input voltage $V_1$ is set at 240, 400, and 480 V, while the output voltage $V_2$ is set at 48 V. The measured $j_{r,\text{rms}}$ for the proposed modulation is smaller compared with that for the VFM + PSM. A similar observation can be obtained when the BSRC is in the reverse mode, as shown in Fig. 17(b). It verifies that the elimination of backflow power by the proposed modulation can reduce the rms value of the resonant current.

D. Measured Efficiency

The measured DC–DC efficiency of the BSRC is shown in Fig. 18. Solid curves represent efficiency for the proposed modulation, while dashed curves represent that for the VFM + PSM. It can be observed from Fig. 18(a) that, with the proposed modulation, the BSRC has better efficiency performance, especially under light load conditions. A similar observation can be obtained when the BSRC is in the reverse mode, as shown in Fig. 18(b). We can also observe that the efficiency in Mode 1 is lower than that in the other modes due to the higher switching frequency, the larger the resonant current, the lower the delivered power. In particular, normalized values rather than real values are used in Fig. 17. In consideration of the based of the normalized current shown in (22), although the normalized value in the pink case is higher than that in the blue case, the real value in pink case is smaller than that in the blue case. Thus, its efficiency could be higher.

Fig. 19 shows the traditional loss breakdown of the BSRC with the proposed modulation and the VFM + PSM. Due to
the elimination of backflow power and reduction of the hard switching actions, the switch and transformer losses for the proposed modulation are smaller than that for the VFM + FSM under different operating settings, which mainly contributes to the efficiency improvement for the proposed modulation.

VI. CONCLUSION

Backflow power is eliminated and switching loss is alleviated for a BSRC with a novel modulation scheme proposed in this article. The proposed modulation is formed by inserting zero voltage level and tuning the operating frequency along with the variation of the gain and the power level. The BSRC can operate in both buck- and boost-like modes for a wide gain range. Moreover, the resonant current can be fully released before the completion of the switching cycle to alleviate the hard turn-off problem. The number of hard switching actions is significantly reduced compared with existing modulation schemes in the literature. The proposed modulation is experimentally validated by a 1 kVA prototype of BSRC.

APPENDIX

The state equations have been given in Section II. In this section, we will discuss the constraint conditions of each working mode to calculate the initial values of the given state equations.

1) Mode 1: The operation during half switching cycle can be divided into three stages. Since the resonant current $j_r$ and voltage $m_r$ are continuous and the operations are symmetrical for positive and negative half cycles, the boundary conditions can be given as follow:

$$j_{r1} = (1 - m_{r0}) \sin \varphi_1$$  \hspace{1cm} (A.1)

$$m_{r1} = (-1 + m_{r0}) \cos \varphi_1 + 1$$  \hspace{1cm} (A.2)

$$0 = (1 - m_{r0} - M) \sin \varphi_1 + j_{r1} \cos \varphi_2 - \varphi_1$$  \hspace{1cm} (A.3)

$$-m_{r0} = (-1 + m_{r0} + M) \cos \varphi_1 + j_{r1} \sin \varphi_2 - \varphi_1 + 1 - M. \hspace{1cm} (A.4)$$

Moreover, the delivered current $j_o$ is calculated as follows:

$$j_o = \frac{1}{\pi} \int_{\varphi_1}^{\varphi_2} j_r d\varphi. \hspace{1cm} (A.5)$$

The uncertainties in state equations can be achieved with (A.1)–(A.5) for a given $D_r$ or $P$.

2) Mode 2: There are 2 stages during half switching cycle. The boundary conditions can be given as follow:

$$0 = (1 - m_{r0} - M) \sin \varphi_1 + j_{r0} \cos \varphi_1$$  \hspace{1cm} (A.6)

$$m_{r1} = (-1 + m_{r0} + M) \cos \varphi_1$$  \hspace{1cm} (A.7)

$$-j_{r0} = (M + m_{r1}) \sin \varphi_2 \varphi_1 + 1 - M$$  \hspace{1cm} (A.8)

$$-m_{r0} = (m_{r1} - M) \cos \varphi_2 + \varphi_1 - m_{r1} + 1 - M. \hspace{1cm} (A.9)$$

Moreover, $\varphi_2 = \pi (f_r/f_s)$, which is decided by the delivered current $j_o$ from the following equation:

$$j_o = \frac{1}{\varphi_2} \left( \int_{\varphi_1}^{\varphi_2} j_r d\varphi - \int_{\varphi_1}^{\varphi_2} j_r d\varphi \right). \hspace{1cm} (A.10)$$

Then the variables can be derived as follow:

$$\varphi_1 = \arcsin \left[ \frac{2M - 1}{2} \sin \varphi_2 \right] + \frac{\varphi_2}{2}$$  \hspace{1cm} (A.11)

$$j_{r0} = -\frac{\sin \varphi_1 \sin (\varphi_2 - \varphi_1)}{\sin \varphi_2}$$  \hspace{1cm} (A.12)

$$m_{r1} = -\frac{\sin (\varphi_2 - \varphi_1)}{\sin \varphi_2} + 1 - M$$  \hspace{1cm} (A.13)

$$m_{r0} = -\frac{\cos \varphi_1 \sin (\varphi_2 - \varphi_1)}{\sin \varphi_2} + 1 - M. \hspace{1cm} (A.14)$$

The duty cycle $D_p$ is up to $f_s$

$$D_p = g(f_s) = \frac{\varphi_2}{2\pi f_s} \hspace{1cm} (A.15)$$

$$\varphi_1 = \frac{\varphi_2}{2} + \arcsin \left[ \frac{2M - 1}{2} \sin \varphi_2 / 2 \right]$$  \hspace{1cm} (A.16)

3) Mode 3: The BSRC works for a half resonant cycle during stage 1 and stage 3. Then the constraint conditions are

$$m_{r1} = 2 - 2M - m_{r0}, \hspace{1cm} (A.17)$$

$$-m_{r0} = 2M - m_{r1}. \hspace{1cm} (A.18)$$

Thus the values can be derived as follow:

$$m_{r1} = 1, \hspace{1cm} m_{r0} = 1 - 2M. \hspace{1cm} (A.19)$$

Moreover, the duty cycle $D_p$ is calculated from $\varphi_1 = \pi$

$$D_p = \frac{f_r}{2f_s}. \hspace{1cm} (A.20)$$

4) Mode 4: There are 4 stages for half switching cycle, the conditions are as follows:

$$j_{r1} = (1 - m_{r0} - M) \sin \varphi_1$$  \hspace{1cm} (A.21)

$$m_{r1} = (-1 + m_{r0} + M) \cos \varphi_1 + 1 - M$$  \hspace{1cm} (A.22)

$$(M + m_{r1}) \sin \varphi_2 = j_{r1} \cos (\varphi_2 - \varphi_1)$$  \hspace{1cm} (A.23)

$$m_{r2} = (m_{r1} + M) \cos (\varphi_2 - \varphi_1) + j_{r1} \sin (\varphi_2 - \varphi_1) - M$$  \hspace{1cm} (A.24)

$$\varphi_2 = \varphi_2 + \pi$$  \hspace{1cm} (A.25)

$$-m_{r0} = 2M - m_{r2}. \hspace{1cm} (A.26)$$

The delivered current $j_o$ is calculated as follows:

$$j_o = \frac{1}{\varphi_2} \left( \int_{\varphi_1}^{\varphi_2} j_r d\varphi - \int_{\varphi_1}^{\varphi_2} j_r d\varphi \right). \hspace{1cm} (A.27)$$

With the help of MATLAB, the state variables at each working mode for a given condition can be achieved.

REFERENCES


