Hybrid Modeling Approach Combining Analytical and Neural Ordinary Differential Equations for Accelerated Simulation of Grid-tied Inverter

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***Abstract*—Fine solving time step is commonly required in the simulation of grid-tied inverters due to the fast inner-loop control and high-frequency switching behavior. However, the dynamics of the grid-tied inverters, especially in a large-scale renewable power farm study, are frequently governed by the slower outer-loop control. The mismatching between the small solving time step and the slow outer loop leads to time-consuming simulations when using conventional numerical methods. While a neural network (NN) can serve as a surrogate for the entire grid-tied inverter, modeling full behaviors still demands large and computationally intensive networks. To address this issue, this paper proposes a hybrid modeling approach for accelerated simulation of the grid-tie inverters. It combines analytical models and neural ordinary differential equations (ODEs). Neural ODE (NODE) is employed to solely represent the inner loop dynamics, eliminating deep or complex networks, while the other components outside the inner loop are retained and analytically represented. This hybridization combines the coarse-step capability of NN-based surrogates with the physical interpretability and efficiency of analytical models. Experimental results demonstrate that the proposed hybrid approach achieves high-fidelity predictions under various disturbances and grid faults while significantly reducing simulation time compared with the conventional methods.**

***Index Terms*—Accelerated Simulation, Analytical, Grid-Tied Inverter, Hybrid, Neural Ordinary Differential Equations**

I. Introduction

THE increasing integration of renewable energy has led to widespread deployment of grid-tied inverters in modern power grids, raising significant concerns about system stability issues[1]. Comprehensive simulations have become essential in grid-tied inverters, which enable performance evaluation and optimization of grid-tied systems under diverse operating conditions [2], [3], [4]. Detailed models are predominantly utilized in conventional stand-alone power electronics converter simulations[5]. These physics-based models, constructed with fundamental circuit theory with precise component parameters, can accurately capture fine-grained characteristics including ripples and thermal effects. Facing faster simulation demands, various simplified models have been developed to speed up the validation, e.g., ideal switching models represent nonlinear components with linear equivalents such as the approximate discrete-time switching model [6], [7], switch-state prediction method [8] and event-driven methods [9]. The switching-function approach further improves simulation efficiency by replacing switching circuits with controlled sources and switching functions, eliminating the need for explicit event handling[10].

However, a microsecond-level time step is required by the high-frequency switching behavior in the aforementioned models, making them computationally intensive in system-level simulations (i.e., those simulations include grids, generators, and converters, and require a long simulation time to observe the system stability). Although circuit averaging and linearization are proposed to address this by focusing on macroscopic characteristics while disregarding periodical switching behaviors [11], [12], the inner and outer loops are still discretized using the same small time step which is determined by the faster inner loop. Since the outer loop typically operates at much lower bandwidth and does not require such fine resolution [13], using an unnecessarily small time step throughout leads to excessive computational effort without proportional gains in accuracy. This inefficiency becomes particularly evident when system behavior is governed primarily by outer loop dynamics, as is often the case in system-level simulations.

Neural network (NN) techniques are a promising solution to this nonlinear modeling issue. In such approaches, computationally intensive iterations with fine time steps are replaced with a single forward propagation with a coarse step[14], [15], enabling significant simulation acceleration [16], [17], [18]. Dealing with an entire converter, various NN architectures for time-domain simulation have been explored, including Convolutional Neural Network (CNN)[19], Long Short-term Memory (LSTM)[17], [20], [21], Nonlinear AutoRegressive eXogenous (NARX) network[22], and Transformers[23]. Some studies combine multiple networks to further improve predictive performance. For example, Ref. [24] proposed a composite NN architecture consisting of CNN, LSTM, and an attention mechanism for data-driven modeling of modular multilevel converters (MMC). Ref. [25] proposed an NN-based modeling approach for a DC-DC converter that empirically

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decomposes the output signals into large transients and small periodic components. A fully connected NN is used to map circuit parameters to system characteristics, while an LSTM combined with a CNN is employed to predict signal features in the compressed latent space.

Unfortunately, the mismatching between the small solving time step and the slow outer loop in grid-tied converters is rarely considered in existing NN-based modeling approaches. Without distinguishing which components truly do not require high temporal resolution, one may carefully design a network and training procedures to learn the full converter dynamics as a whole. As a result, unnecessarily complex and overparameterized networks may be introduced due to complicated behaviors brought by various disturbances subjected to a grid-tied inverter, including load changes, control strategy transitions, short-circuit faults and so on [26]. This ultimately undermines the computational efficiency gains that NN-based surrogates are intended to deliver[27], [28].

Leveraging the bandwidth separation between the fast inner and the slow outer loop, a hybrid modeling approach that combines analytical models with neural ordinary differential equations (NODEs) to accelerate simulations is proposed in this paper. Unlike existing NN-based modeling approaches, the proposed approach does not replace the whole converter with an NN-based surrogate model but rather focuses on the computationally intensive components.

As illustrated in Fig. 1, this paper employs a NODE model to represent the computationally intensive switch-based components and the fast inner current loop, not only due to its excellent compatibility with existing simulation methods but also because of its strong potential for accelerating simulations [29]. First, the NODE model predicts the derivatives of the states rather than the states themselves, and the propagation is handled by numerical solvers commonly embedded in major simulation software. This allows the NODE model to be easily integrated into existing inverter simulations. Second, since physical systems like inverters are inherently described by states and their derivatives, using NODE to fit the relationship between the two will be closer to the physical nature. Physical information can be indirectly introduced into the training process, enhancing predictive performance without the need to prudently design a deep or complicated network. Moreover, unlike conventional RNNs and LSTMs that explicitly store and update hidden states within the network, NODE delegates trajectory generation to the ODE solver and only parameterizes the local derivative field. Therefore, its kernel network can remain structurally simple, and a fully connected NN is sufficient for this modeling task without introducing additional hidden-state layers to store temporal information.

The other components of the inverter under the proposed approach are retained in analytical form. Specifically, an equivalent variable current source is designed to replace the switch-based chopper circuit based on averaging techniques, while the slow outer loop remains analytically modeled. Thus, the grid-tied control strategies implemented in the outer loop are analytically expressed and interpretable. It makes the proposed model adapt to a wide range of grid-tied conditions while retaining computational efficiency.

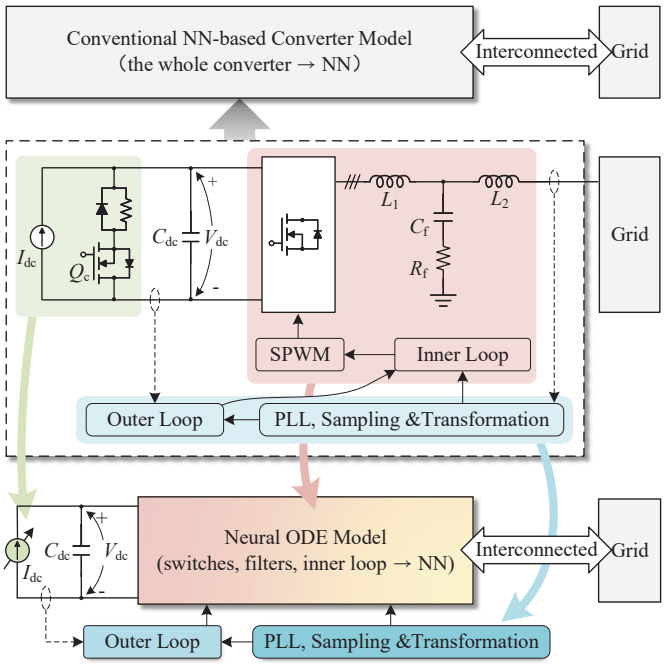

Fig. 1. Conventional NN-based time-domain modeling approaches and the proposed hybrid modeling approach of a grid-tied inverter.

The main contribution of this paper is the proposal of a hybrid modeling framework for grid-tied inverters aimed at accelerating simulations. The framework is constructed based on the different bandwidths of the components in an inverter and partitions them according to algebraic constraints. In particular, within the proposed framework, algebraic constraints are incorporated into the design of the NODE model. Only data related to the inner loop dynamics is required, avoiding the need to exhaustively sample across diverse grid-tied conditions of the entire inverter. Furthermore, the algebraic constraints make the NODE model focus solely on capturing the fast inner loop dynamics, rather than modeling the entire inverter. This leverages the large-step advantage of neural networks while avoiding the need for deep or complex architectures. Computational cost estimation confirms that the proposed hybrid model maintains a low parameter count and runtime burden, comparable to that of both the averaged model and the switch-based model.

The remainder of this paper is organized as follows: Chapter II introduces the grid-tied three-phase inductor-capacitor-inductor (LCL) inverter and the proposed hybrid modeling approach. Chapter III gives the modeling and training process of the NODE model. Chapter IV implements the hybrid model in MATLAB/Simulink and verifies the computational cost and accuracy. Chapter V concludes this paper.

II. Hybrid Modeling of Grid-tied Three-Phase LCL Inverters

This paper takes a grid-tied three-phase LCL inverter as the modeling case, which is widely used in renewable energy generation. The inverter adopts a common grid-tied current inner-loop control strategy, while the outer-loop consists of DC-side and grid-side voltage control. A low voltage ride

through (LVRT) strategy and chopper circuit is implemented to protect against grid faults in the inverter[30]. Since this paper focuses on the system-level behaviors modeling, the detailed characteristics like heat and parasitic effect are omitted. The switch-based model of the inverter is built based on the ideal switches and passive components. The parameters of the passive components are time-invariant and the same in the three phases. The grid is ideal with a balanced three-phase. The following subsections introduce the topology and control strategies of the grid-tied three-phase LCL inverter and the proposed hybrid modeling approach.

A. Topology and Parameters of the Grid-tied Three-phase LCL Inverter

The topology and the control block diagram of the inverter are shown in Fig. 2. The ordinary differential equations (ODEs) of the main power circuit are given in abc-axis as follows:

$$L_1\frac{di_{1k}}{dt} = e_k - R_1 i_{1k} - v_{ck}, \tag{1a}$$
$$C_f\frac{dv_{ck}}{dt} = i_{1k} - i_{2k}, \tag{1b}$$
$$L_2\frac{di_{2k}}{dt} = v_{ck} - R_2 i_{2k} - v_{gk}, \tag{1c}$$
$$C_{dc}\frac{dV_{dc}}{dt} = \frac{P_{in} - \sum v_{gk} i_{2k}}{V_{dc}}, \tag{1d}$$

where

$$e_k = (2S_k - 1)\frac{V_{dc}}{2}, \tag{2a}$$
$$S_k(t) \in \{0, 1\}, \tag{2b}$$

$k = a, b, c$. e_k are the inverter terminal voltages, which are rectangular waveforms generated by the sinusoidal pulse width modulation (SPWM). S_k are switching states of each phase leg. i_{1k} is the inverter-side filter inductor current. v_{ck} are the filter capacitor voltage. i_{2k} represents the grid-side filter inductor current. v_{gk} denote the grid voltage. V_{dc} is the DC-bus voltage. I_{dc} is the input current governed by a controllable current source. $P_{in} = V_{dc} I_{dc}$ is the input power of the inverter. Q_1 - Q_6 are the ideal switches under switching frequency f_s. Q_c is the ideal switch in the chopper circuit. R_c is the power-consuming resistor. L_1 and L_2 are the inverter-side and grid-side filter inductors. R_1 and R_2 are the resistors in the filter inductors. C_f is the filter capacitor. R_f is the passive damping resistor. C_{dc} is the DC-bus capacitor. Equations (1) are usually transformed to the dq-axis as follows:

$$L_1\frac{\mathrm{d}I_{1d}}{\mathrm{d}t} = E_d - RI_{1d} - V_{cd} + \omega_g L_1 I_{1q}, \tag{3a}$$
$$L_1\frac{\mathrm{d}I_{1q}}{\mathrm{d}t} = E_q - RI_{1q} - V_{cq} - \omega_g L_1 I_{1d}, \tag{3b}$$
$$C_f\frac{\mathrm{d}V_{cd}}{\mathrm{d}t} = I_{1d} - I_{2d} + \omega_g C_f V_{cq}, \tag{3c}$$
$$C_f\frac{\mathrm{d}V_{cq}}{\mathrm{d}t} = I_{1q} - I_{2q} - \omega_g C_f V_{cd}, \tag{3d}$$
$$L_2\frac{\mathrm{d}I_{2d}}{\mathrm{d}t} = V_{cd} - RI_{2d} - V_{gd} + \omega_g L_2 I_{2q}, \tag{3e}$$
$$L_2\frac{\mathrm{d}I_{2q}}{\mathrm{d}t} = V_{cq} - RI_{2q} - V_{gq} - \omega_g L_2 I_{2d}, \tag{3f}$$
$$C_{dc}\frac{\mathrm{d}V_{dc}}{\mathrm{d}t} = \frac{P_{in} - V_{gd}I_{2d} - V_{gq}I_{2q}}{V_{dc}}, \tag{3g}$$

where E_d and E_q are the inverter terminal voltages transformed from e_k under Clarke-Park transformation while they are represented as follows:

$$E_d = m_d\frac{V_{dc}}{2}, \tag{4a}$$
$$E_q = m_q\frac{V_{dc}}{2}, \tag{4b}$$

where $m_d, m_q \in [0, 1]$ are the modulation signals in dq-axis. I_{1d} and I_{1q} are the inverter-side filter inductor current. V_{cd} and V_{cq} are the filter capacitor voltage. I_{2d} and I_{2q} represent the grid-side filter inductor current. V_{gd} and V_{gq} denote the grid voltage. $\omega_g = 2\pi f_g$ is the grid angular frequency as f_g is the grid frequency. The state variables mentioned in this paragraph are all described in the dq-axis.

The current inner-loop control functions are given as follows:

$$V_{d,m} = (K_{p,in} + K_{i,in}/s)(I_{2d,ref} - I_{2d}) + V_{gd} - \omega_g L_f I_{2q}, \tag{5a}$$
$$V_{q,m} = (K_{p,in} + K_{i,in}/s)(I_{2q,ref} - I_{2q}) + V_{gq} + \omega_g L_f I_{2d}, \tag{5b}$$

where $V_{d,m}$ and $V_{q,m}$ (the units are V) represent the terminal voltage reference signals of the inverter in the dq-axis. s represents the Laplace variable. $I_{2d,ref}$ and $I_{2q,ref}$ (the units are A) are the grid-side inductor reference currents given by the outer loop. $K_{p,in}$ and $K_{i,in}$ are the dimensionless proportional and integral gains of the inner-loop discrete PI controller with sampling time $T_{s,in}$. $L_f = L_1 + L_2$ is the total inductance of the LCL filter.

DC-side and grid-side voltage control strategies are implemented in the outer-loop control. The control functions are expressed as follows:

$$I_{2d,ref} = (K_{p,dc} + K_{i,dc}/s)(V_{dc} - V_{dc,ref}), \tag{6a}$$
$$I_{2q,ref} = (K_{p,ac} + K_{i,ac}/s)(V_{ac,ref} - V_{ac}). \tag{6b}$$

where $V_{dc,ref}$ and $V_{ac,ref}$ (the units are V) are the reference DC-bus voltage and AC voltage. $K_{p,dc}$, $K_{i,dc}$, $K_{p,ac}$, and $K_{i,ac}$ are the dimensionless proportional and integral gains of the discrete outer-loop proportional–integral (PI) controller with sampling time $T_{s,out}$. V_{ac} is defined as the three-phase grid voltage magnitude as follows:

$$V_{ac} = \sqrt{\frac{v_{ga}^2 + v_{gb}^2 + v_{gc}^2}{3}} * \frac{1}{\sqrt{2}}. \tag{7}$$

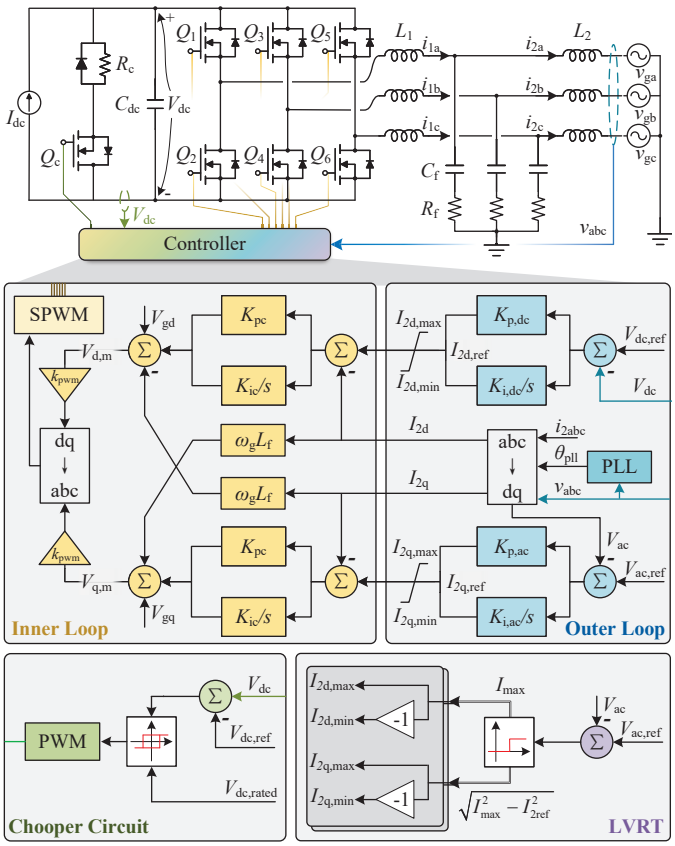

Fig. 2. Topology and control block diagram of a grid-tied three-phase LCL inverter.

Phase-locked loop (PLL) is described by the following differential equations:

$$\frac{\mathrm{d}\theta_{\mathrm{pll}}}{\mathrm{d}t} = \omega_{\mathrm{g}} + V_{\mathrm{gq}}(K_{\mathrm{p,pll}} + K_{\mathrm{i,pll}}/s). \tag{8}$$

where θ_{pll} is the estimated phase angle of the grid voltage generated by PLL, $K_{\mathrm{p,pll}}$ and $K_{\mathrm{i,pll}}$ are the dimensionless proportional and integral gains of the PLL.

During LVRT, the integrators in the outer loop are frozen as the grid voltage dips over a threshold, and the outer loop output currents are limited to the maximum current threshold $I_{\max}$. The control priority shifts from active current to reactive current to support grid voltage. The maximum current relationship between $I_{\mathrm{2d,ref}}$ and $I_{\mathrm{2q,ref}}$ is given as follows:

$$I_{\mathrm{2d,max}} = \begin{cases} I_{\max}, m = 0 \\ \sqrt{I_{\max}^2 - I_{\mathrm{2q,ref}}^2}, m = 1 \end{cases} \tag{9a}$$

$$I_{\mathrm{2q,max}} = \begin{cases} I_{\max}, m = 1 \\ \sqrt{I_{\max}^2 - I_{\mathrm{2q,ref}}^2}, m = 0 \end{cases} \tag{9b}$$

$$I_{\mathrm{2d,min}} = -I_{\mathrm{2d,max}} \tag{10a}$$

$$I_{\mathrm{2q,min}} = -I_{\mathrm{2q,max}} \tag{10b}$$

$$m = \begin{cases} 0, |V_{\mathrm{ac}} - V_{\mathrm{ac,ref}}| < 0.05 \\ 1, |V_{\mathrm{ac}} - V_{\mathrm{ac,ref}}| \geq 0.05 \end{cases} \tag{11}$$

To prevent excessive DC-bus voltage rise, a switch-based chopper circuit is introduced on the DC side. The chopper works on a hysteresis band, i.e., activates when the DC-bus voltage exceeds $1.05 \times V_{\mathrm{dc,rated}}$ ($V_{\mathrm{dc,rated}}$ is the rated DC-bus voltage) and turns off when it drops below $1.025 \times V_{\mathrm{dc,rated}}$. It is worth noting that the switch-based chopper circuit is also computationally demanding due to its pulse width modulation (PWM), which requires a small simulation time step. Moreover, it introduces additional nonlinearities into the inverter, making NN modeling of the entire inverter particularly challenging. The key parameters of the aforementioned components are listed in Table I.

TABLE I
PARAMETERS OF THE THREE-PHASE GRID-TIED LCL INVERTER.

Symbol	Description	Value
Main Power Circuit		
f_{s}	Switch frequency	5kHz
L_1	Inverter Side Filter Inductor	1.8×10^{-4}H
L_2	Grid Side Filter Inductor	3.5×10^{-4}H
C_{f}	Filter Capacitor	9.099×10^{-5}F
R_{f}	Passive Damping Resistor	$5 \times 10^{-4}\Omega$
C_{dc}	DC-bus Capacitor	0.03F
Inner Loop		
$K_{\mathrm{p,in}}$	Proportional Gain	1.2
$K_{\mathrm{i,in}}$	Integral Gain	40
$T_{\mathrm{s,in}}$	Sampling Time	$5 \times 10^{-5}s$
Outer Loop		
$K_{\mathrm{p,dc}}, K_{\mathrm{p,ac}}$	Proportional Gain	5
$K_{\mathrm{i,dc}}, K_{\mathrm{i,ac}}$	Integral Gain	50
$T_{\mathrm{s,out}}$	Sampling Time	$2 \times 10^{-4}s$
$I_{\max}$	Maximum Current	4000A
Chopper Circuit		
R_{c}	Dissipative resistor	2Ω
$V_{\mathrm{dc,ref}}$	Reference DC-bus Voltage	2000V
$V_{\mathrm{dc,rated}}$	rated DC-bus Voltage	2000V
PLL		
$K_{\mathrm{p,pll}}$	Proportional Gain	20
$K_{\mathrm{i,pll}}$	Integral Gain	200

B. Proposed Hybrid Modeling Approach

The proposed hybrid modeling approach exploits the inherent disparity in bandwidth between different components. In a typical power electronics converter, the outer loop demonstrates significantly lower bandwidth compared to the inner loop. This observation motivates employing a NN to capture the fast dynamics of the inner loop, switches, and the filters since they are coupled, while maintaining analytical models for components that exhibit slower dynamics and minimal impact on simulation speed. The proposed hybrid model comprises three key parts as illustrated in Fig. 3:

1) A NODE model that replaces the switches, filters, and inner loop which exhibit fast dynamics.
2) An equivalent variable current source representing the switch-based chopper circuit and input power characteristics using an averaging technique.
3) Analytical parts for the remaining components, including the DC-bus capacitor, outer loop, and PLL.

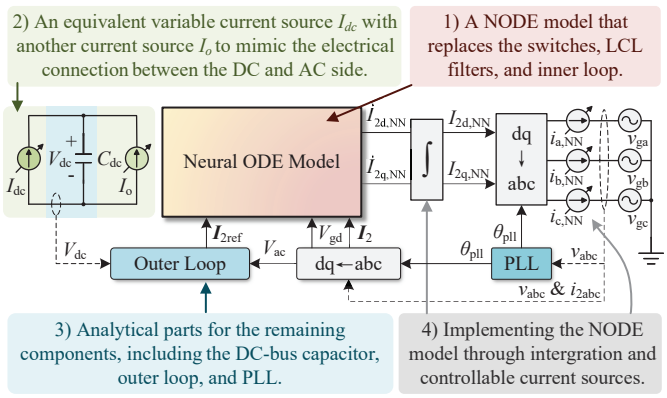

Fig. 3. The structure of the proposed hybrid model.

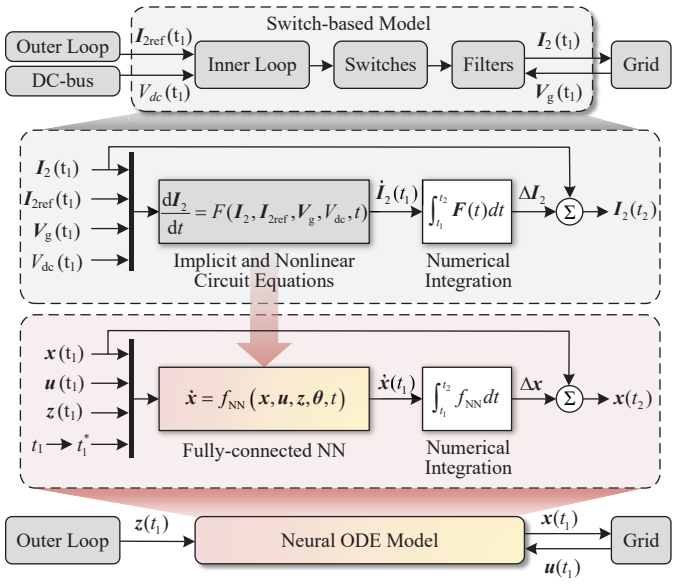

Fig. 4. The NODE model replaces the fast inner loop, highly nonlinear switches, and LCL filters with a fully-connected NN.

The grey part in Fig. 3 illustrates that the NODE model is implemented in a function block with integration and controllable sources. The NODE model predicts the derivatives of $\boldsymbol{I}_2$, i.e., $\dot{I}_{2\mathrm{d,NN}}$ and $\dot{I}_{2\mathrm{q,NN}}$, which are integrated to $I_{2\mathrm{d,NN}}$ and $I_{2\mathrm{q,NN}}$. Then they are transformed back to abc-axis $i_{\mathrm{a,NN}}, i_{\mathrm{b,NN}}, i_{\mathrm{c,NN}}$. I_{dc} is the input current of the DC side. I_{o} is the output equivalent current of the DC-bus which will be introduced in the following detailed introduction of the three key parts:

1) **The NODE model**: Previously, NODE is proposed to replace the kernel function F in the numerical integration with a fully-connected NN f_{NN}[32], given as:

$$\dot{\boldsymbol{x}} = F(\boldsymbol{x}, t) \rightarrow \dot{\boldsymbol{x}} = f_{\mathrm{NN}}(\boldsymbol{x}, \boldsymbol{\theta}, t) \tag{12}$$

where f_{NN} represents a NN that maps the relationship between the states and their derivatives with $\boldsymbol{\theta}$ which are the weights and bias parameters of the NN. The kernel NN f_{NN} doesn't predict the states directly, but the derivative of the states. Thus, the physical evolution information is introduced indirectly into the NN by the forward propagation with a numerical solver. In our prior work[29], external inputs and time-encoding techniques are introduced to enhance the predicting performance of the NODE framework in power electronic converter modeling. Since the NODE model in this paper contains parts of the inverter but not the whole, the algebraic constraints between the NN part and the analytical parts are considered and embedded into the NODE model to enhance the predictive performance further, as given as follows:

$$\dot{\boldsymbol{x}} = f_{\mathrm{NN}}(\boldsymbol{x}, \boldsymbol{\theta}, t) \rightarrow \dot{\boldsymbol{x}} = f_{\mathrm{NN}}(\boldsymbol{x}, \boldsymbol{z}, \boldsymbol{u}, \boldsymbol{\theta}, t) \tag{13}$$

where $\boldsymbol{x}$, $\boldsymbol{z}$, and $\boldsymbol{u}$ are the states, algebraic variables, and external inputs of the modeled parts. In physics-based modeling, it is easy to obtain the following relationship by combining (3a)-(3f), (4), and (5), which is generally summarized by:

$$\frac{\mathrm{d}\boldsymbol{I}_2}{\mathrm{d}t} = F(\boldsymbol{I}_2, \boldsymbol{I}_{2\mathrm{ref}}, \boldsymbol{V}_{\mathrm{g}}, V_{\mathrm{dc}}, t) \tag{14}$$

where $\boldsymbol{I}_2 = [I_{2\mathrm{d}}, I_{2\mathrm{q}}]^\top$ and $\mathrm{d}\boldsymbol{I}_2/\mathrm{d}t$ are the states and the derivative of the grid-side inductors, $\boldsymbol{V}_{\mathrm{g}} = [V_{\mathrm{gd}}, V_{\mathrm{gq}}]^\top$ are the external grid voltage input, $\boldsymbol{I}_{2\mathrm{ref}} = [I_{2\mathrm{d,ref}}, I_{2\mathrm{q,ref}}]^\top$ are the algebraic variables obtained from the outer-loop controller, F is the mapping relationship between the states and their derivation, external inputs, algebraic variables and time in original Switch-based model. Leveraging the structural similarity between the neural network f_{NN} in (13) and the original function F in (14), Fig. 4 illustrates how the function F can be replaced by a neural network f_{NN}. Specifically, this paper utilized NODE (13) to replace (3a)-(3f), (4) and (5), while (3g) and (6)-(11) remain analytically expressed. The detailed implementation of the NODE model will be elaborated in Section III.

2) **The equivalent variable current source**: The switch-based chopper circuit and the input power are modeled as an equivalent variable current source based on the averaging method, which is governed by:

$$I_{\mathrm{dc}} = \frac{P_{\mathrm{in}}}{V_{\mathrm{dc}}} - k_{\mathrm{chop}} \frac{V_{\mathrm{dc}}}{R_{\mathrm{c}}} \tag{15}$$

where k_{chop} turns into 1 when V_{dc} exceeds $V_{\mathrm{dc,rated}}$ by 5%, and turns into 0 when it drops below 2.5%. Since the implementation of NODE inherently decouples the electrical connection of DC and AC subsystems, another controllable current source is added to the output side of the DC-bus capacitor to maintain the power balance. The controllable current source I_{o} is expressed as follows:

$$I_{\mathrm{o}} = \frac{3}{2} \frac{V_{\mathrm{gd}} I_{2\mathrm{d}} + V_{\mathrm{gq}} I_{2\mathrm{q}}}{V_{\mathrm{dc}}} \tag{16}$$

3) **The analytical parts**: The DC-bus capacitor, outer loop, and PLL are still constructed in the analytically expressed model as given in (3g), (6)-(10).

Within this partitioning strategy, NN resources focus on modeling the most challenging nonlinear and fast inner loop dynamics, while the remaining components retain physically interpretable analytical models. It eliminates the need for a

deep or complex NN to carry both outer and inner loop dynamics, while maintaining crucial physical insights into the inverter's operation.

III. Implementation of the NODE Model

The implementation of the NODE model including the definition of the inputs and outputs, the generation of the dataset, the configuration of the model and the training. Then, the NODE model is exported from PyTorch and implemented in MATLAB/Simulink. The process is illustrated in Fig. 5 and detailed in the following sections.

Firstly, the selection of inputs and outputs for the NN-based kernel function necessitates a definition of the modeled subsystem within the inverter while maintaining proper algebraic relationships with other components. In the case of this paper, since the NODE model replaces the inner loop, switches, and filters, the subsystem is naturally defined as the state variables and algebraic variables of the inner loop and the filters, which are in touch with other components directly. According to (14), the grid-side inductor currents $\boldsymbol{I}_2$ are treated as the states, and its derivatives are determined by $\boldsymbol{I}_2$, $\boldsymbol{I}_{2\text{ref}}$, $\boldsymbol{V}_\text{g}$ and V_dc. Thus, to ensure the structure similarity, $\boldsymbol{I}_2$ are selected as the output states of the NODE model, while the reference currents $\boldsymbol{I}_{2\text{ref}}$ from the outer loop are chosen as the algebraic variables, $\boldsymbol{V}_\text{g}$ and V_dc are selected as external inputs:

$$\begin{cases} \mathbf{u}(t)_{\text{input1}} = [V_\text{gd}(t), V_\text{dc}(t)] \\ \mathbf{z}(t)_{\text{inputs2}} = [I_{2\text{d,ref}}(t), I_{2\text{q,ref}}(t)] \\ \mathbf{x}(t)_{\text{outputs}} = [I_{2\text{d}}(t), I_{2\text{q}}(t)] \end{cases} \tag{17}$$

Notably, only the d-axis grid voltage V_gd is selected as the external input but not $\boldsymbol{V}_\text{g}$. The reason is that the q-axis grid voltage V_gq is zero in an ideal balanced three-phase system with proper PLL operation. This paper aims to verify the hybrid ability and simulation effectiveness of the proposed method, thus non-ideal grid is not considered. Such a subsystem definition based on algebraic constraints restricts the learning space of the NODE model to the inner loop. This excludes the nonlinear dynamics of the outer loop, DC side, and chopper circuit, thereby eliminating the need to generate datasets that cover all possible grid-tied scenarios typically governed by the outer loop.

The switch-based numerical model of the inverter is built in Simulink 2024b based on *Simscape Electrical Specialized Power Systems Library* for generating a dataset. The subjected power through controllable current source I_dc is given as:

$$I_\text{dc} = \frac{k_1 P_\text{in}}{V_\text{dc}} \tag{18}$$

where P_in is fixed at 4MW. Meanwhile, inputs are generated as:

$$V_\text{gd} = 200k_2 \times [1 + k_3 \times 0.4 \times \sin(2\pi k_8 t)] + 700 \tag{19a}$$

$$I_{2\text{d,ref}} = \frac{2P_\text{in}}{3V_\text{gd}} \times [k_4 + 0.4 \times k_5 \times \sin(2\pi k_9 t)] \tag{19b}$$

$$I_{2\text{q,ref}} = [k_6 + 0.4 \times k_7 \times \sin(2\pi k_{10} t)] \times 4000 \tag{19c}$$

where $k_1, k_2, ..., k_{10}$ are srandom numbers generated differently in each simulation. To prevent excessive current in the inverter when the grid voltage is low, potentially leading to an excessively high d-axis current, the following constraint is imposed on the inner loop reference signal:

$$\sqrt{I_{2\text{d,ref}}^2 + I_{2\text{q,ref}}^2} \le I_\text{max} \tag{20}$$

The dataset is generated by randomly updating the $k_1, k_2, ..., k_{10}$ every 0.15s and each simulation runs for 3s with a fixed time step of 1e-6s, using the Euler solver. A total of 180 simulations are conducted, with data downsampled by the sample rate 1×10^5 Hz, resulting in a complete dataset size of

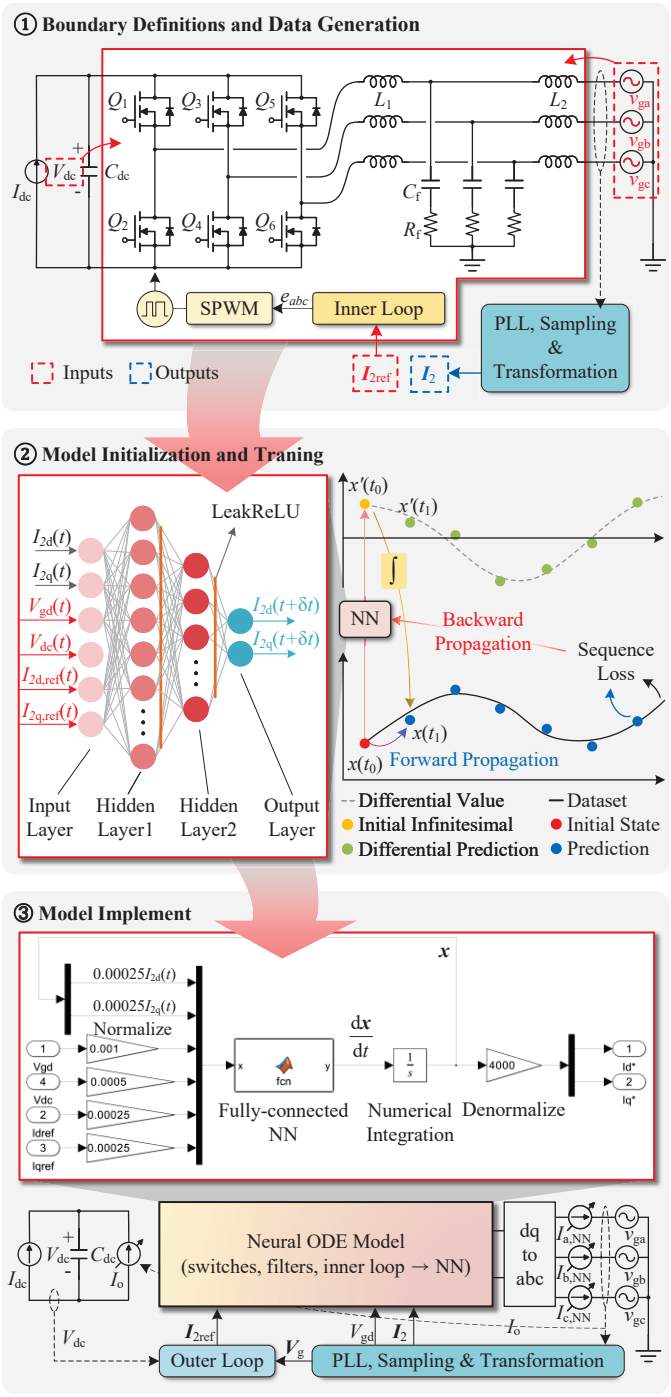

Fig. 5. The modeling process of the NODE model.

$540 \times 1e5 \times 6$. The input and output signals are stored in MAT 7.3, with a total file size of approximately 1.88 GB, storing states (not the derivatives) for further processing and model training.

Notably, this paper employs a simulation-based dataset instead of experimental measurements from a physical inverter due to the following considerations:

1) This paper primarily focuses on modeling the system-level inner-loop dynamics of the inverter. The fine-grained switching behaviors of power semiconductor devices (e.g., switches and diodes), which are inherent in hardware implementations, have limited influence on large-signal behavior and system-level dynamic analysis [31].
2) Advanced commercial techniques for handling measurement noise are now widely available and can effectively suppress noise without introducing significant distortions in system-level transient responses. Therefore, this paper assumes that the noise has been well-treated, while noise filtering algorithms are beyond the scope of this paper.
3) In addition, the boundary signals (i.e., the input and output of the NN defined in the proposed approach) are commonly available in practical digital controllers. The measured ports of the simulated inverter can be readily applied to a physical one.

In short, whether the data originate from simulations or physical inverters does not affect the validity or effectiveness of the proposed modeling approach. Hence, simulation is selected as a more efficient means of generating training data.

Next, the Torchdiffeq repository[32] based on the PyTorch platform is modified to support variable input signals, temporal encoding and mini-batch gradient descent, implementing the enhanced NODE models. During training, the NODE model predicts a sequence using a numerical solver. The loss is computed by comparing the predicted states sequence with the dataset but not the direct derivatives. The loss is then backpropagated through the network. The hyperparameters of training are summarized in Table II.

TABLE II
TRAINING HYPERPARAMETERS OF THE NODE MODEL.

Hyperparameters	Settings
Forward Propagation Method	fourth-order Runge-Kutta
Backward Propagation Method	Gradient Descent
Batch Size	128
Loss Function	MSE
Sequence Length	5
Interval	5
Iteration	100000
Initial Learning Rate	2e-3
Optimizer	Adam
Learning Decay Rate	0.99
Decay Step	100
Neurons in Hidden Layer 1	48 (LeakReLU)
Neurons in Hidden Layer 2	24 (LeakReLU)

The weights, biases, and activation functions of the trained NODE model are exported from PyTorch and integrated into Simulink using a MATLAB function block, as shown in Fig. 5. The NN-generated output currents, $I_{2d,NN}$ and $I_{2q,NN}$, are produced through forward propagation by feeding the reference current signals $I_{2d,ref}$ and $I_{2q,ref}$ from the outer loop, along with the grid voltage V_{gd} and the DC-bus voltage V_{dc}, into the NODE model. These output currents are applied to controllable current sources, transformed into the abc-axis, and then injected into the grid.

IV. EXPERIMENTAL VALIDATION

This section analyzes the computational cost of the proposed hybrid model against the switch-based numerical model and the averaged model. Then, the predictive performance of the proposed hybrid model is evaluated under various fault conditions.

A. Computational Cost Comparison

Floating-point operations (FLOPs) serve as the primary metric when comparing the switch-based numerical model, the averaged model, and the proposed hybrid model. The FLOP counting methodology follows these conventions: Basic arithmetic operations (addition, subtraction, multiplication) consume 1 FLOP. Division consumes 2 FLOPs. Trigonometric functions consume 10 FLOPs. Note that actual computational costs for division and trigonometric operations may vary depending on hardware implementation and software optimizations. The models were implemented in MATLAB using a fourth-order Runge-Kutta (RK4) solver, with computational cost comparisons presented in Table III.

TABLE III
ESTIMATED FLOPS OF THE SWITCH-BASED NUMERICAL MODEL, THE AVERAGED MODEL AND THE PROPOSED HYBRID MODEL.

Model	Numerical Model	Averaged Model	Proposed Hybrid Model
Time Step	1×10^{-6}s	5×10^{-5}s	2×10^{-4}s
FLOPs Per Step	454	356	3328
Simulation Time	2s	2s	2s
Total FLOPs	3.62×10^{9}	5.70×10^{7}	1.33×10^{8}
CPU Time	45.5770s	0.1272s	0.0704s

For fair benchmarking, the FLOPs calculation excludes external operations such as function calls, logical comparisons, memory access, and numerical solver routines. Each model is executed five times, and the CPU time is averaged. Results show that the proposed hybrid model requires more FLOPs per time step than the switch-based numerical model. The former's computational overhead primarily stems from its forward propagation of the NN. However, its superior numerical stability enables operation with a significantly coarser time step, resulting in overall computational efficiency gains. The averaged model shows the lowest cost overhead, but its practical application is often limited by the proprietary nature of commercial inverter designs, for example, constraints on the small sampling period of the discrete inner loop controller and switching period. Note that the averaged model consumes the lowest FLOPs, but the proposed hybrid model costs less time. This result might be attributed to the underlying optimization of matrix operations in Basic Linear Algebra Subprograms

TABLE IV
PREDICTIVE ACCURACY VALIDATION RESULTS OF THE PROPOSED HYBRID MODEL UNDER COMMON GRID-TIED CONDITIONS.

Fault Types	Evaluated Period	Relative Root Mean Square Error (rRMSE)				
		Active Power P	Reactive Power Q	DC-bus Voltage V_{dc}	D-axis Current $I_{2\text{d}}$	Q-axis Current $I_{2\text{q}}$
Three-phase short circuit	0.8-2.0s	0.0654	0.3900	0.0054	0.0858	0.0713
Single-phase short circuit	0.95-1.8s	0.0139	0.0991	0.0012	0.0192	0.0922
Power fluctuations	0.8-2.75s	0.0090	1.4452	0.0005	0.0090	1.4453
Grid voltage drop	0.7-2.3s	0.0070	0.0890	0.0003	0.0070	0.0872
Grid voltage rise	0.9-1.6s	0.0069	0.1297	0.0003	0.0069	0.1325
DC-bus disturbance (96%)	1.3-2.2s	0.0081	1.5004	0.0006	0.0081	1.5004
Low DC-bus voltage (85%)	1.3-2.2s	0.0208	1.3615	0.0025	0.0114	1.4184
Power fluctuations under Low DC-bus voltage	0.8-2.75s	0.0266	1.4371	0.0019	0.0266	1.4371

(BLAS) and Linear Algebra PACKage (LAPACK) provided by Matlab. Considering that neural networks are essentially matrix operations and the running step size can be larger, although the total FLOPs of neural networks is higher than that of average models, the running time is still shorter.

B. Predictive Accuracy Evaluation under Fault and Disturbance Tests

The proposed hybrid NODE model's predictive accuracy is evaluated through three common power system variables: active power (P) and reactive power (Q) at the point of common coupling, along with DC-bus capacitor voltage (V_{dc}). Meanwhile, the grid-side inductor currents $I_{2\text{d}}$ and $I_{2\text{q}}$ are also monitored to exhibit the direct predictive results of the hybrid NODE model. The initial power range from 1 MW to 4 MW was evenly divided into 48 steady-state points to minimize randomness and ensure the robustness of the testing outcomes. The simulation setup employs initial conditions of 2000V for the DC-bus capacitor and 900V (Peak Value) for the 50Hz grid voltage, while other state variables are initialized as zero. Once the initial condition is provided, the switch-based numerical model along with the averaged model and the proposed hybrid model, will generate the state sequences under the numerical solver[33]. The simulations are conducted under a fixed-step Euler solver to avoid solver-dependent multi-stage evaluations and highlight the time cost of the models themselves. The step sizes are configured as the same in Table III. Multiple operational scenarios including several fault conditions and disturbances are conducted. The quantitative evaluated results are presented in Table IV. Fig. 6 and Fig. 7 illustrated some examples of the evaluation results. The left y-axis in Fig. 6 and 7 represented the measured physical quantity, while the right y-axis corresponded to the absolute error between the proposed model and the numerical model for the same variable. The following are the details of the conducted tests:

1) **Short circuit fault:** Three-phase and single-phase short-circuit faults are applied at $t = 1\,\text{s}$, with a duration of $0.15\,\text{s}$. The proposed hybrid model demonstrates high-fidelity tracking of both transient and post-fault recovery dynamics, as evidenced by the comparative waveforms in Fig. 6(a), 6(b), 7(a), and 7(b).
2) **Power fluctuations:** The input power is reduced from 3.8MW to 1.4MW at t = 1-1.5s, then increased back to 3.8MW at t = 2-2.5s. Despite these step changes, the proposed hybrid model maintains accurate prediction, as shown in Fig. 6(c) and Fig. 7(c).
3) **Grid Voltage Drop:** A 5% grid voltage drop was introduced at t = 1s and sustained for 1s before being cleared. The experimental results are shown in Fig. 6(d) and Fig. 7(d).
4) **Grid Voltage Rise:** A 5% grid voltage rise was applied at t = 1s and cleared 0.3s later. The experimental results, presented in Fig. 6(e) and Fig. 7(e). It highlights an important observation: the training dataset does not contain instances where the grid voltage exceeds 900V. Despite this, the proposed hybrid model successfully predicts the transient response, demonstrating its acceptable generalization capabilities beyond the training data range.
5) **DC-bus disturbance (96%):** A 4% drop in DC-bus voltage occurs at t = 1.5s, lasting 0.5s. The model exhibits strong predictive accuracy as shown in Fig. 6(f) and Fig. 7(f).
6) **Low DC-bus Voltage (85%):** A 15% drop in DC-bus voltage occurs at t = 1.5s. The model still exhibits well predictive accuracy as shown in Fig. 6(g) and Fig. 7(g).
7) **Power fluctuations under low DC-bus voltage:** The input power is reduced from 3.8MW to 1.4MW at t = 1-1.5s, then increased back to 3.8MW at t = 2-2.5s under 85% DC-bus voltage. The model exhibits good predictive accuracy despite variations in reference values, as shown in Fig. 6(i) and Fig. 7(i).
8) **Amplitude-phase characteristics:** The closed-loop characteristics of the proposed hybrid model is evaluated under 5% $V_{\text{dc,ref}}$ and V_{gd} disturbance in 0.8MW as shown in Fig. 8. The results show that the model can accurately predict the transient response of the inverter under DC and AC side small disturbances.

The predictive accuracy evaluated results of the proposed hybrid model's predictive performance is summarized in the Table IV with Relative Root Mean Square Error (rRMSE) between the switch-based numerical model and the proposed hybrid model. Each operating condition was evaluated at 48 evenly distributed steady-state operating points between 1 MW and 4 MW to minimize the potential randomness associated with model prediction accuracy at any single operating point.

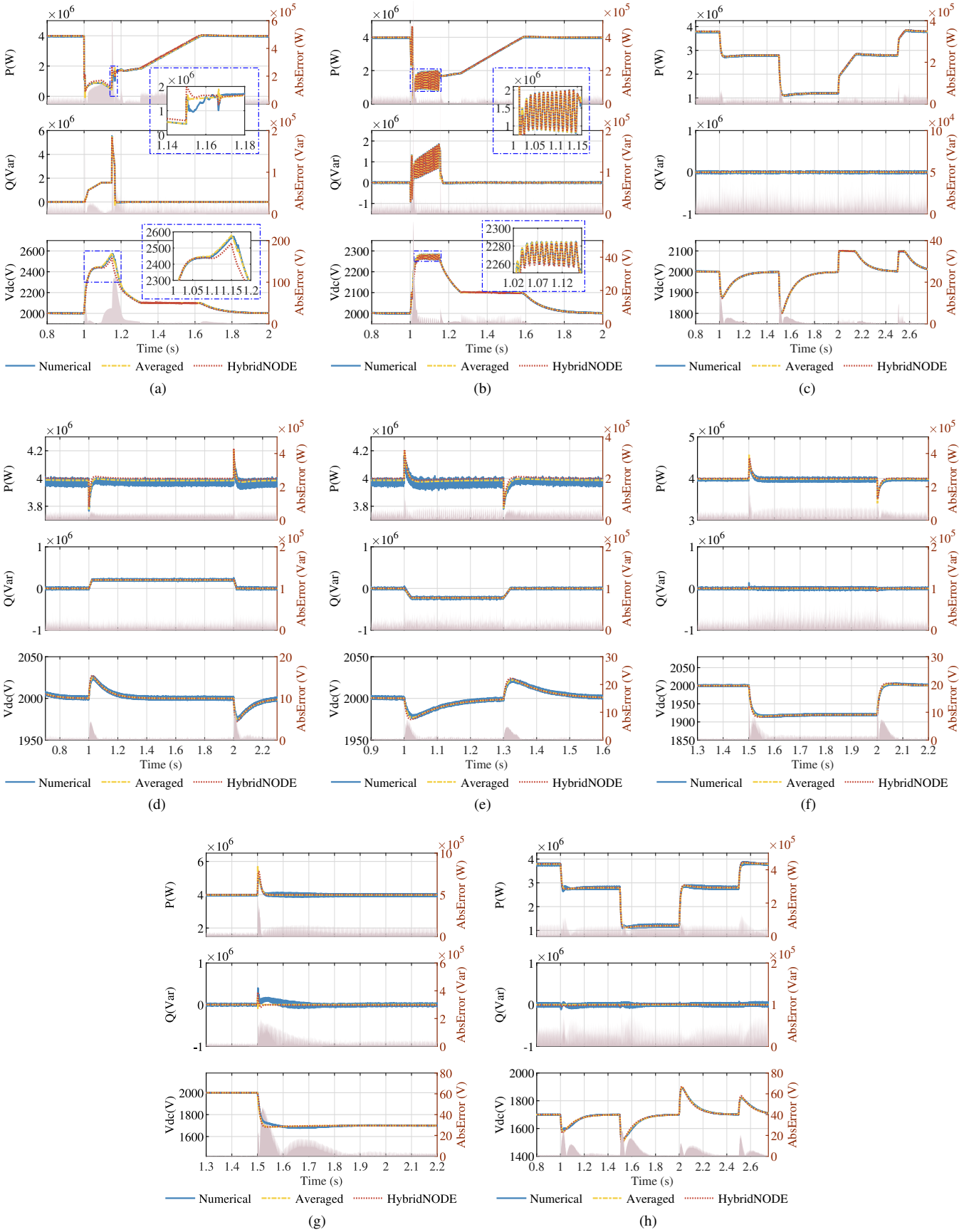

Fig. 6. Predictive power P, Q and DC-bus voltage V_{dc} evaluated results of fault and disturbance tests on the proposed hybrid model: (a) Three-phase short circuits. (b) Single-phase short circuit. (c) Power fluctuations. (d) Grid voltage drop. (e) Grid voltage rise. (f) DC-bus disturbance (96% drop). (g) Low DC-bus voltage (85% drop). (h) Power fluctuations under low DC-bus voltage.

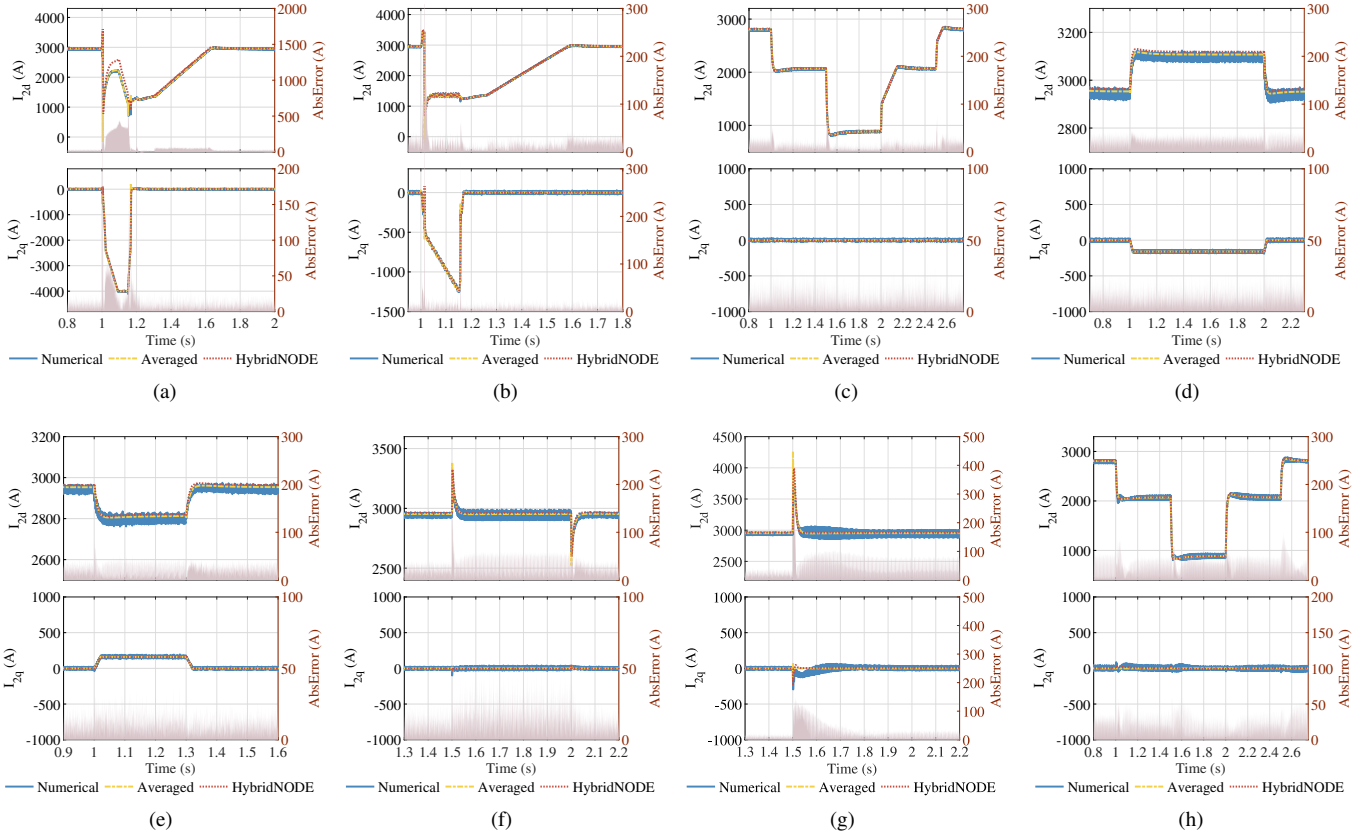

Fig. 7. Predictive current I_{2d} and I_{2q} evaluated results of fault and disturbance tests on the proposed hybrid model. (a) Three-phase short circuits. (b) Single-phase short circuit. (c) Power fluctuations. (d) Grid voltage drop. (e) Grid voltage rise. (f) DC-bus disturbance (96% drop). (g) Low DC-bus voltage (85% drop). (h) Power fluctuations under low DC-bus voltage.

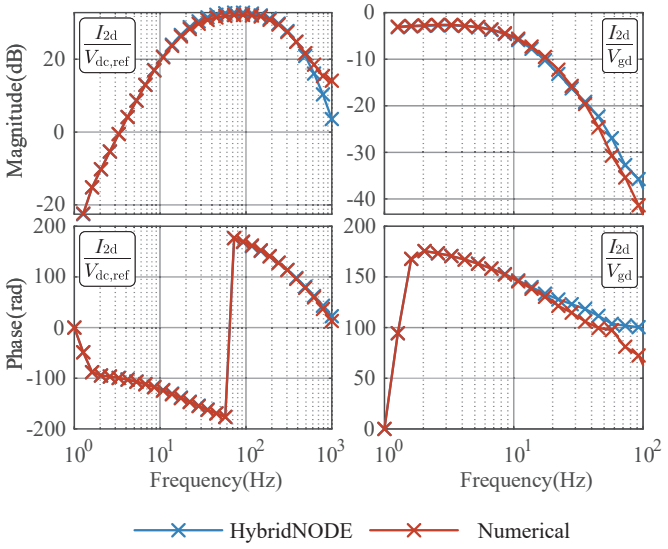

Fig. 8. Validation results on amplitude-phase characteristics of the proposed hybrid model.

The rRMSE is calculated as follows:

$$\text{rRMSE} = \frac{\sqrt{\frac{1}{N}\sum_{i=1}^{N}(y_i - \hat{y}_i)^2}}{\bar{y}_i} \tag{21}$$

where y_i and $\hat{y}_i$ denote the actual dataset values and the corresponding NN predictions, respectively; $\bar{y}_i$ is the mean of the actual data, and N is the number of samples. Since the proposed hybrid model is evaluated with a larger time step, linear interpolation is applied to the NN-predicted values to ensure consistency in vector length with the reference dataset. The results demonstrate the high fidelity of the proposed hybrid model in predicting system dynamics under various fault and disturbance conditions. It should be clarified that rRMSE greater than 1 for reactive power in the power fluctuations and DC-bus disturbance tests does not indicate poor performance of the proposed hybrid model. This occurs because the reactive power remains near zero in these scenarios. Since rRMSE is calculated based on the mean value of the actual dataset, as given in (21), a near-zero mean leads to a relatively large rRMSE.

C. Comparison on the Measured CPU Time and CPU Usage in Real-time Simulation

The CPU time is recorded over five runs and averaged. Results in the Table V show that the proposed hybrid model requires significantly less CPU time, which is only 1-2% of that required by the switch-based numerical model. This demonstrates substantial computational time savings while maintaining high prediction fidelity.

Furthermore, the real-time simulation based on the proposed hybrid model is conducted[34]. The real-time simulating per-

TABLE V
MEASURED CPU TIME OF THE SWITCH-BASED NUMERICAL MODEL, THE AVERAGED MODEL AND THE PROPOSED HYBRID MODEL IN COMMON GRID-TIED SIMULATIONS.

Fault Types	Measured CPU Time		
	Numerical Model	Averaged Model	Proposed Hybrid Model
Three-phase short circuit	52.123s	1.530s	0.753s
Single-phase short circuit	52.102s	1.507s	0.749s
Power fluctuations	52.413s	1.554s	0.763s
Grid Voltage Drop	51.820s	1.584s	0.777s
Grid Voltage Rise	52.591s	1.553s	0.789s
DC-bus disturbance (96%)	53.018s	1.642s	0.765s
Low DC-bus voltage (85%)	53.995s	1.608s	0.776s
Power fluctuations under low DC-bus voltage	53.063s	1.559s	0.792s

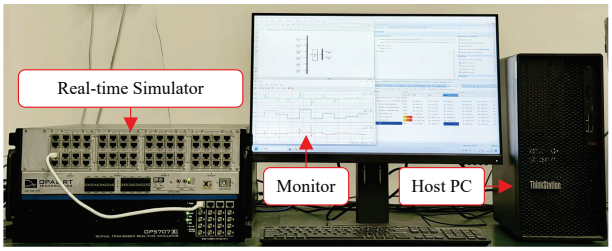

Fig. 9. OPAL-RT real-time simulation platform used for testing the CPU usage of the proposed hybrid model.

formance is evaluated based on OPAL-RT 5707XG real-time simulator platform, as presented in Fig. 9. Considering that the proposed hybrid model is designed to model the inner-loop control, switches and the filters of the original switch-based numerical model, to ensure a fair computational usage comparison, simulations only on the CPU are conducted on the real-time simulation platform. The CPU usage percentage during simulations is recorded from the "Monitor" panel suggested by OPAL-RT. The results are summarized in Table VI. The proposed hybrid model demonstrates a significant reduction in CPU usage, requiring only 2-3% of the CPU resources compared to the switch-based numerical model under time step 2×10^{-4}s. Even in the same time step, the proposed hybrid model still consumes about 81.4% of the CPU resources of the switch-based numerical model. This highlights the proposed hybrid model's potential for real-time applications, enabling efficient and accurate simulations of grid-tied inverters.

TABLE VI
MEASURED CPU USAGE OF THE SWITCH-BASED NUMERICAL MODEL AND THE PROPOSED HYBRID MODEL ON OPAL-RT REAL-TIME SIMULATOR.

Model	Numerical Model	Proposed Hybrid Model	Proposed Hybrid Model
Time Step	1×10^{-5}s	1×10^{-5}s	2×10^{-4}s
Total CPU usage	10.74%	8.75%	0.49%

V. CONCLUSION

This paper proposes a hybrid modeling approach combining analytical and neural ordinary differential equations (ODEs) for accelerated simulation of grid-tied inverters. The approach employs a neural ODE (NODE) model to represent the computationally intensive switch-based components, while keeping the remaining components analytical. This significantly reduces computational cost and enables faster simulation while maintaining high accuracy without relying on deep or complicated networks. Estimated floating-point operations (FLOPs) in MATLAB show that the proposed hybrid model incurs substantially lower computational cost compared to conventional switch-based models, resulting in a reduction of three orders of magnitude in computational time. Further experiments implemented in Simulink demonstrated the high predictive accuracy of the hybrid model under various fault and disturbance scenarios. CPU time measurements indicated that the proposed model requires only 1-2% of the simulation time compared to the switch-based model.

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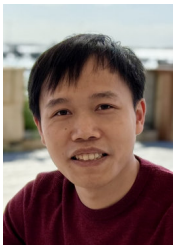

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